FORTEC
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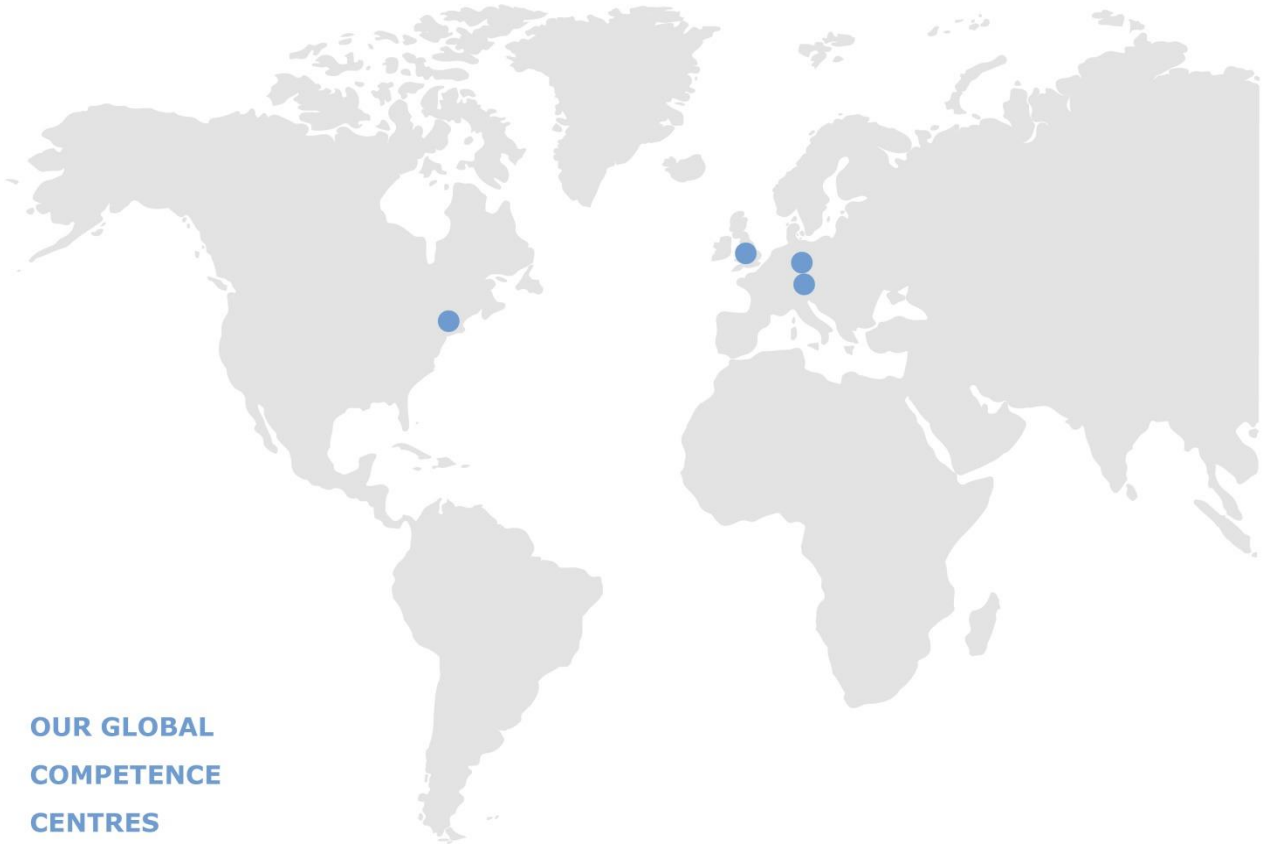

OUR GLOBAL COMPETENCE CENTRES

APOLLO DISPLAY TECHNOLOGIES

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DISPLAY TECHNOLOGY

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Datasheet

ORTUSTECH

COM104H9M11

OR-20-042

Specifications for

Blanview TFT-LCD Monitor (PLAN)

Version 0.3

MODEL G9M11

ORTUSTECH

所属長	検印	担当
'21.03.19	'21.03.19	平山

Version History

Ver.	Date	Page	Description	
0.1	Oct 16, 2020	-	-	First issue
0.2	Dec 23, 2020	10 12	-	Added description of recommended 17-pin and 18-pin inputs for LVDS 6-bit. PWM frequency standard value change.
0.3	Mar 19, 2021	10	-	LVDS 6-bit explanation added.

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1. Application

2. Outline Specifications

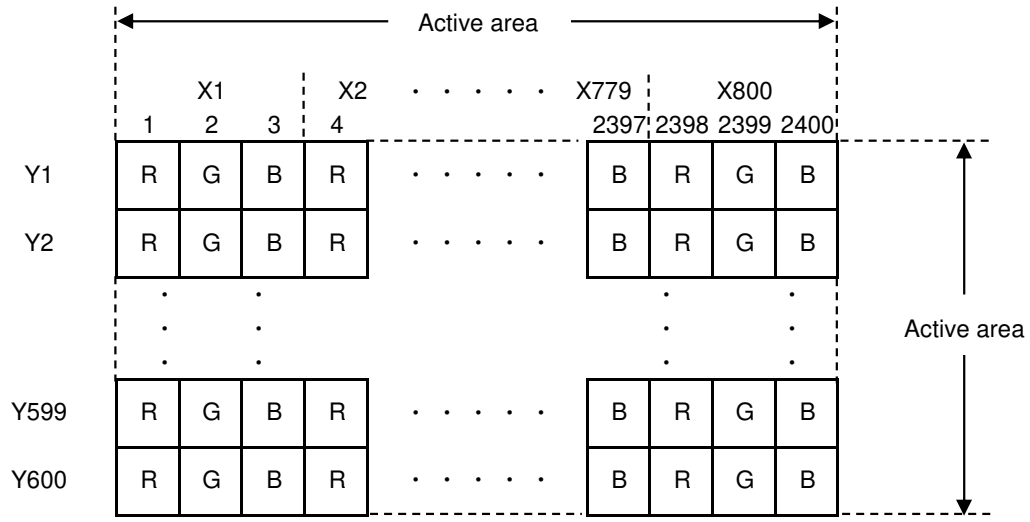
2.1 Features of the Product

- 10.4 inch diagonal display, 800 x RGB [H] x 600 [V] dots.
- 16.7 Million colors / 262 thousand colors.
- Timing generator [TG], Counter-electrode driving circuitry, Built-in power supply circuit.
- High bright white LED back-light, Built-in backlight drive circuit.
- Blanview TFT-LCD, improved outdoor readability.

	Indoor		Outdoor	
	Readability	Power Efficiency (Battery Life)	Readability	Power Efficiency (Battery Life)
Transmissive	Good	Good	Fair	Poor
Transflective	Fair	Poor	Good	Good
Blanview	Good	Good	Good	Good

2.2 Display Method

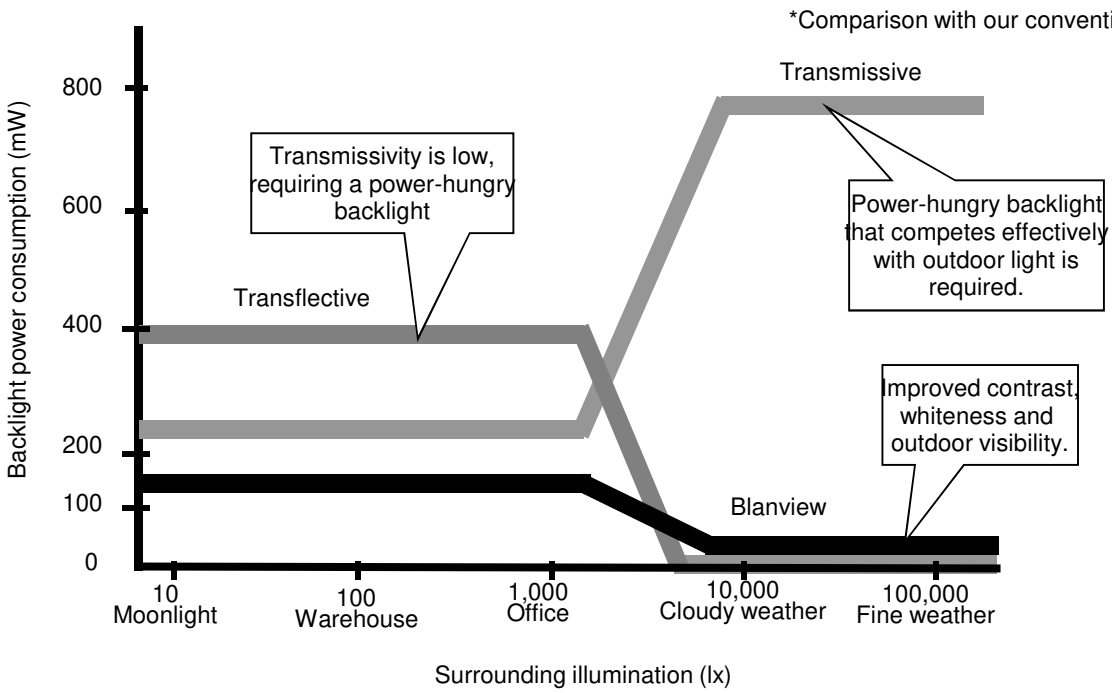
Items	Specifications	Remarks
Display type	FFS 16.7 Million colors / 262 thousand colors. Blanview, Normally black.	
Driving method	a-Si TFT Active matrix. Line-scanning, Non-interlace.	
Dot arrangement	RGB stripe arrangement.	Refer to "Dot arrangement"
Signal input method	VESA/JEIDA LVDS Interface.	
Backlight type	High bright white LED.	
NTSC ratio		



Dot arrangement(FPC is right side.)

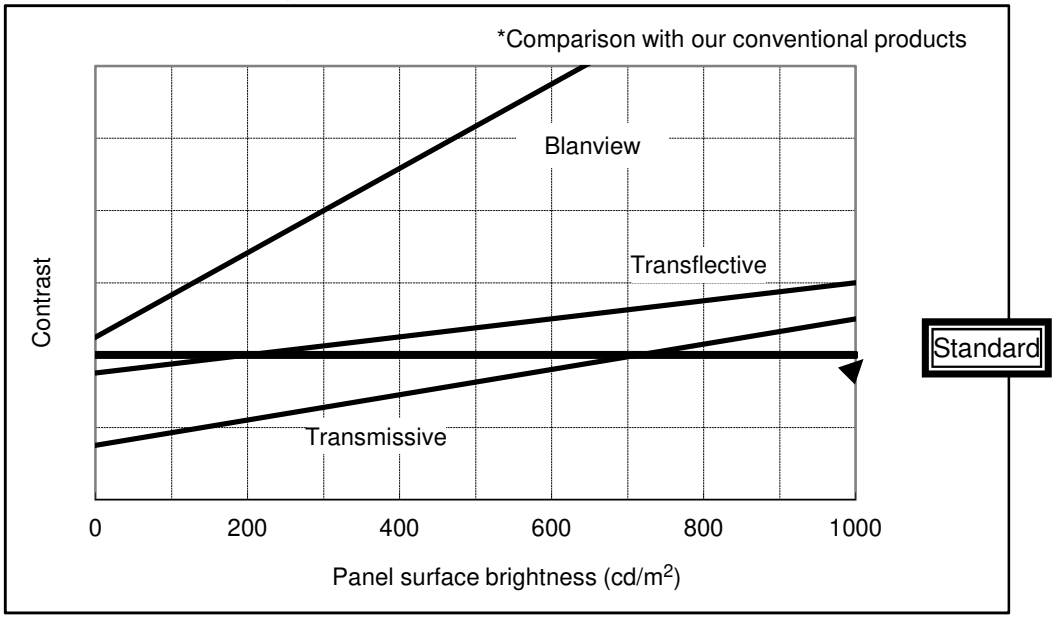
<Features of Blanview>

- Backlight power consumption required to assure visibility. (equivalent to 3.5"QVGA)



- Contrast characteristics under 100,000lx.（same condition as direct sunlight.）

With better contrast (higher contrast ratio), Blanview TFT-LCD has the best outdoor readability in three different types of TFT-LCD.
Below chart shows contrast value against panel surface brightness. (Horizontal: Panel surface brightness/ Vertical: Contrast value) LCD panel has enough outdoor readability above our Standard line.
(TOPPAN PRINTING criteria)



3. Dimensions and Shape

3.1 Dimensions

Items	Specifications	Unit	Remarks
Outline dimensions	(230.0)[H] × (180.2)[V] ×(11.0)[D]	mm	Exclude FPC and
Active area	211.2[H] × 158.4[V]	mm	Diagonal 264.0 mm
Number of dots	2400[H] × 600[V]	dot	
Dot pitch	88.0[H] × 246.0[V]	um	
Weight	T.B.D.	g	Include FPC cable

3.2 Outward Form

Fig. 2 Outline drawing

3.3 Serial No. print (S-print)

T.B.D

4. Pin Assignment

LCD_CN

No.	Symbol	Details
1	VCC	Power supply (3.3V)
2	VCC	Power supply (3.3V)
3	GND	Ground
4	GND	Ground
5	R0-	LVDS DATA0(-)
6	R0+	LVDS DATA0(+)
7	GND	Ground
8	R1-	LVDS DATA1(-)
9	R1+	LVDS DATA1(+)
10	GND	Ground
11	R2-	LVDS DATA2(-)
12	R2+	LVDS DATA2(+)
13	GND	Ground
14	CLK-	LVDS CLK(-)
15	CLK+	LVDS CLK(+)
16	GND	Ground
17	R3-	LVDS DATA3(-) *Note
18	R3+	LVDS DATA3(+) *Note
19	MODE	VESA/JEIDA switching terminal (Low: 8bit_JEIDA or 6bit_JEIDA / High: 8bit_VESA)
20	SC	Display direction switching (Low: Normal display, High: Reverse display)

- Used connector: 20186-020E-11F (I-PEX) or FI-SEB20P-HFE (JAE)
- Corresponding connector: 20197-*20U-F (I-PEX) or FI-S20S[for discrete Wire], FI-SE20ME[for FPC] (JAE)

Note) For 6-bits input, set MODE = 0 (JEIDA) and set pin numbers 17, 18 as the following recommended inputs.
- Enter GND at 17 and 18.
  or
- Enter the Low data of the LVDS transmitter in 17 and 18.
  or
- Connect pin 17 to VCC via 680Ω-10kΩ and pin 18 to GND via 620Ω-10kΩ.

BL_CN

No.	Symbol	Details	Remark
1	VL	Backlight Voltage (12V)	
2	VL	Backlight Voltage (12V)	
3	GNDL	Ground	
4	GNDL	Ground	
5	BLEN	Backlight ON-OFF	High: ON Low: OFF
6	VPDIM	Light Dimmer Control (PWM) input	High active

- Used connector: FI-S6P-HFE (JAE)
- Corresponding connector: FI-S6S (JAE)

- Please make sure to check a consistency between pin assignment in "3.2 Outward Form" and your connector pin assignment when designing your circuit.
  Inconsistency in input signal assignment may cause a malfunction.

5. Absolute Maximum Rating

Item	Symbol	Rating		Unit
		MIN	MAX	
LCD Supply Voltage	VCC	-0.3	4.0	V
Input Voltage for Logic	VI	-0.3	VCC+0.3	V
Backlight Power Supply Input Voltage	VL	-0.3	14.0	V
Backlight ON-OFF	BLEN	-0.3	14.0	V
Light Dimmer Control (PWM) input Voltage	VPDIM	-0.3	5.75	V
Operational temperature range Note1	Top	-30	70	℃
Storage temperature range	Tstg	-30	80	℃

Note1: Panel surface temperature

6. Characteristics

6.1 DC Characteristics

6.1.1 LCD Display Module

(Unless otherwise noted, Ta=25 ℃,VCC=3.3V,GND=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
LCD Supply Voltage	ICC		(3.0)	3.3	(3.6)	V	VCC
LCD operating current	ICC		-	TBD	TBD	mA	VCC
Allowable ripple voltage	VRP	VCC=+3.3V	-	-	TBD	mVp-p	VCC
Input Voltage for Logic	LCD_VIH		0.8×VCC	-	VCC	V	MODE, SC
	LCD_VIL		0	-	0.2×VCC	V	MODE, SC

6.1.2 Backlight

(Unless otherwise noted, Ta=25 ℃,VL=12V,GND=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Supply Input Voltage	VL		(10.8)	12.0	(13.2)	V	VL
Supply Input Current	IL		--	TBD	TBD	mA	VL
Supply Input Rush Current	ILR	VL=12.0V	--	--	TBD	A	VL(Reference)
Backlight ON-OFF	High_BLEN	ON	(2.5)	--	(VL)	V	BLEN
	Low_BLEN	OFF	0	--	(0.4)	V	
Light Dimmer Control PWM Input Voltage	Low_VPDIM	ON	(2.5)	--	(5.5)	V	VPDIM
	High_VPDIM	OFF	0	--	(0.4)	V	
PWM frequency	f PDIM		200	500	1000	Hz	VPDIM
Dimming Rate (PWM Duty)	DR	VL=12.0V	(5)	--	100	%	VPDIM
Estimated Life of LED Note	LL	IL=(45)mA Ta=25℃	--	(70,000)	--	hrs	

Note: - The lifetime of the LED is defined as a period till the brightness of the LED decreases to the half of its initial value.
- This figure is given as a reference purpose only, and not as a guarantee.
- This figure is estimated for an LED operating alone. As the performance of an LED may differ when assembled as a monitor together with a TFT panel due to different environmental temperature.
- Estimated lifetime could vary on a different temperature and usually higher temperature could reduce the life significantly.

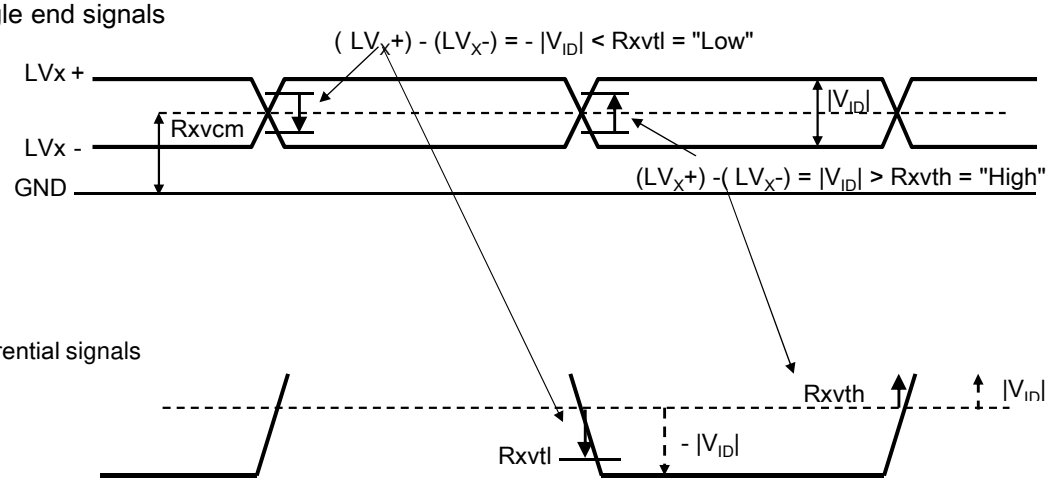
6.2 LVDS Interface

6.2.1 LVDS DC Characteristics

(Unless otherwise noted, Ta=25 ℃,VCC=3.3V,GND=0V)

Item	Symbol	Condition	Rating			Unit	Applicable terminal
			MIN	TYP	MAX		
Differential input high threshold	Rxvth	R_{XVCM}=1.2V	-	-	0.1	V	CLK+, CLK- R0+, R0-, R1+, R1- R2+, R2-, R3+, R3-
Differential input low threshold	Rxvtl		-0.1	-	-	V	
Differential input Common-mode voltage	Rxvcm		0.6	1.2	2.4-|VID|/2	V	
Differential input voltage	$\|V_{ID}\|$		0.2	0.4	0.6	V	
Differential input leakage current	RVXliz		-10	-	10	uA	

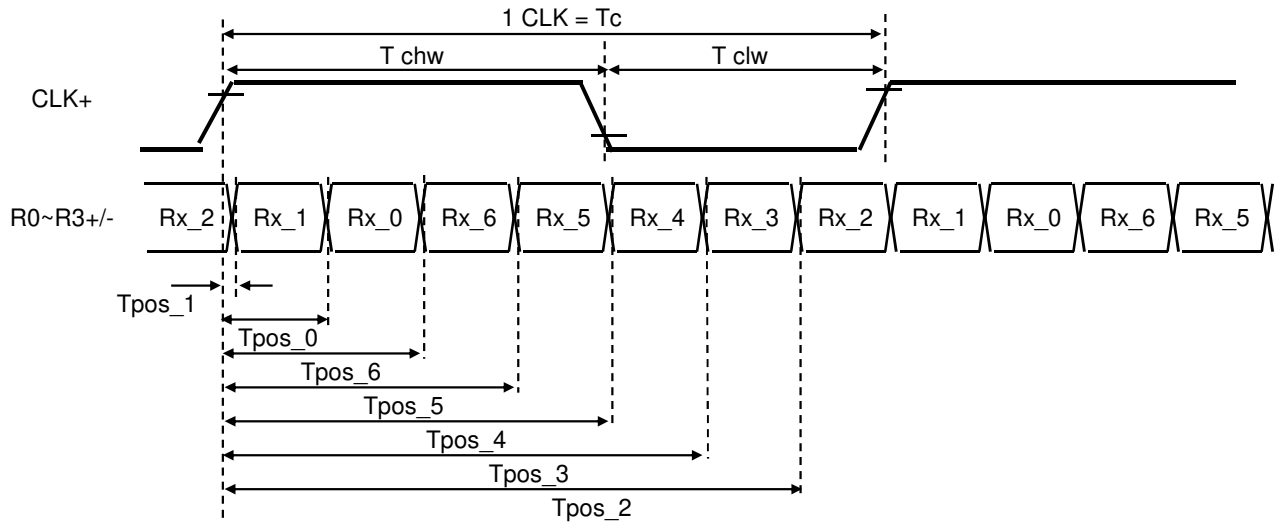
Single end signals

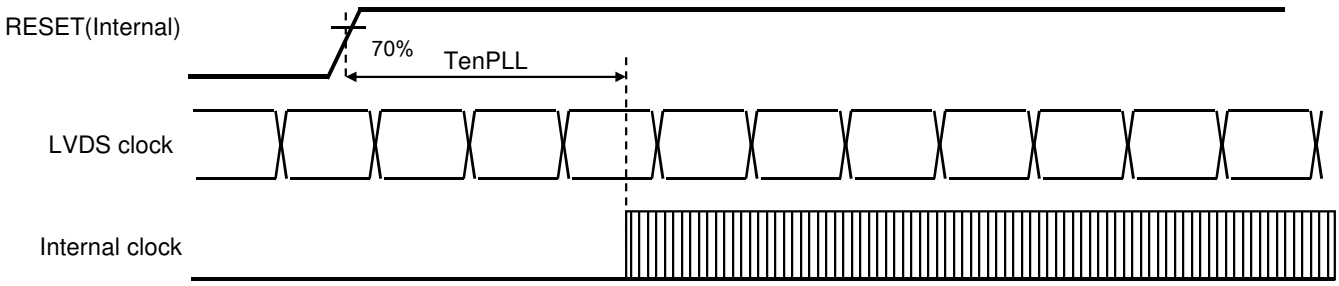


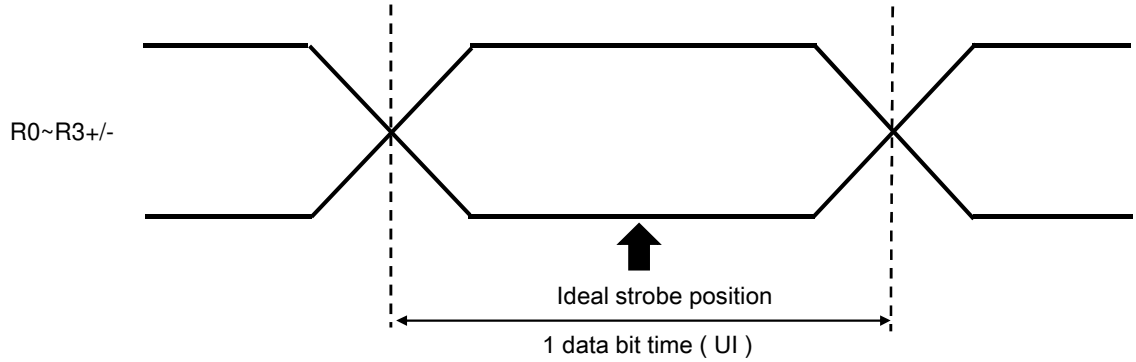
6.2.2 LVDS AC Characteristics

(Unless otherwise noted, Ta=25 ℃,VCC=3.3V,GND=0V)

Item	Symbol	Rating			Unit	
		MIN	TYP	MAX		
CLK Frequency	f clk	20	-	80	MHz	
Clock period	Tc	12.5	-	50	ns	
1 data bit time	UI	-	1/7	-	Tc	
CLK High level Width	T chw	-	4	-	UI	
CLK Low level Width	T clw	-	3	-	UI	
Position 1	Tpos_1	-0.25	0	0.25	UI	
Position 0	Tpos_0	0.75	1	1.25	UI	
Position 6	Tpos_6	1.75	2	2.25	UI	
Position 5	Tpos_5	2.75	3	3.25	UI	
Position 4	Tpos_4	3.75	4	4.25	UI	
Position 3	Tpos_3	4.75	5	5.25	UI	
Position 2	Tpos_2	5.75	6	6.25	UI	
PLL wake-up time	TenPLL	-	-	150	us	

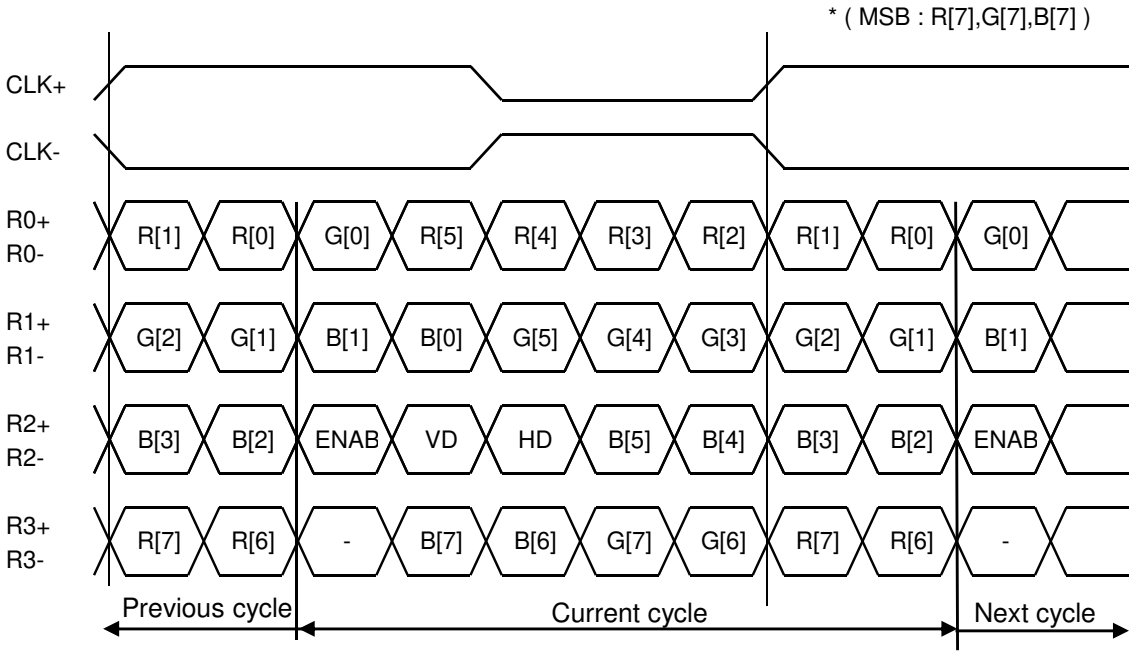




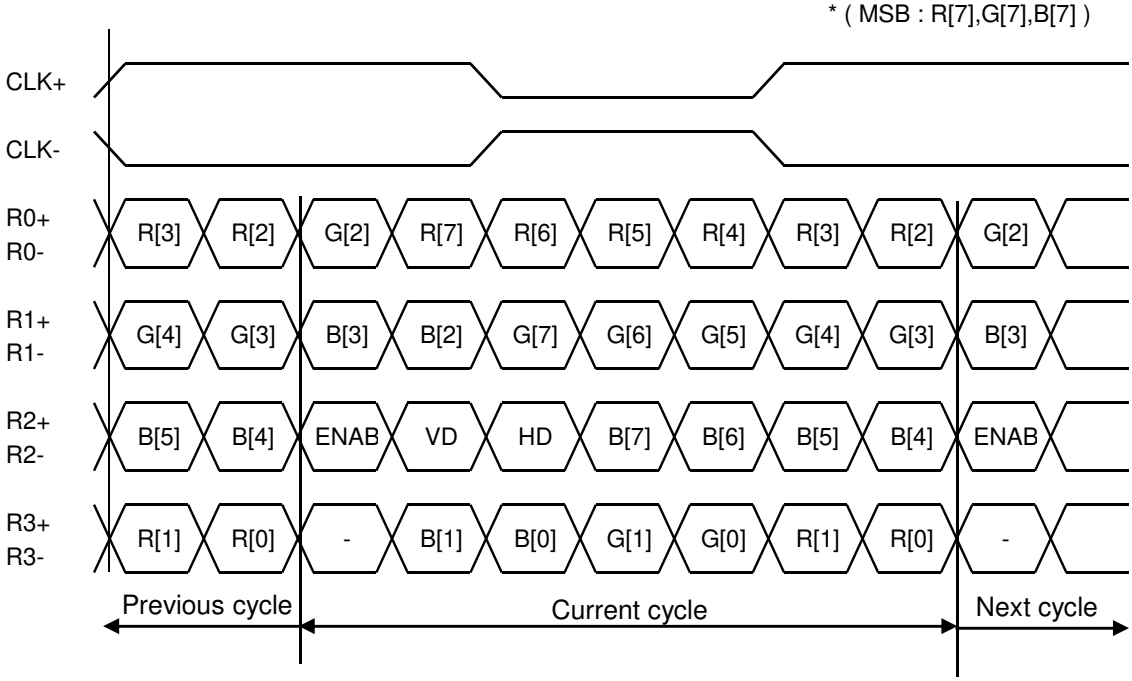


6.2.3 Input Data Format

VESA Format 8bit (MODE = High)



JEIDA Format 8bit (MODE = Low)

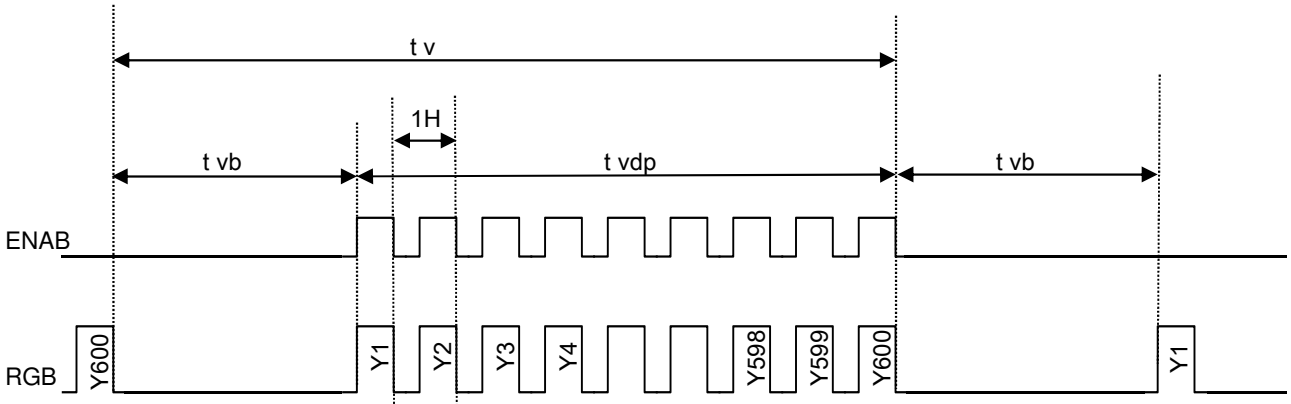


6.3 Input Timing Specifications

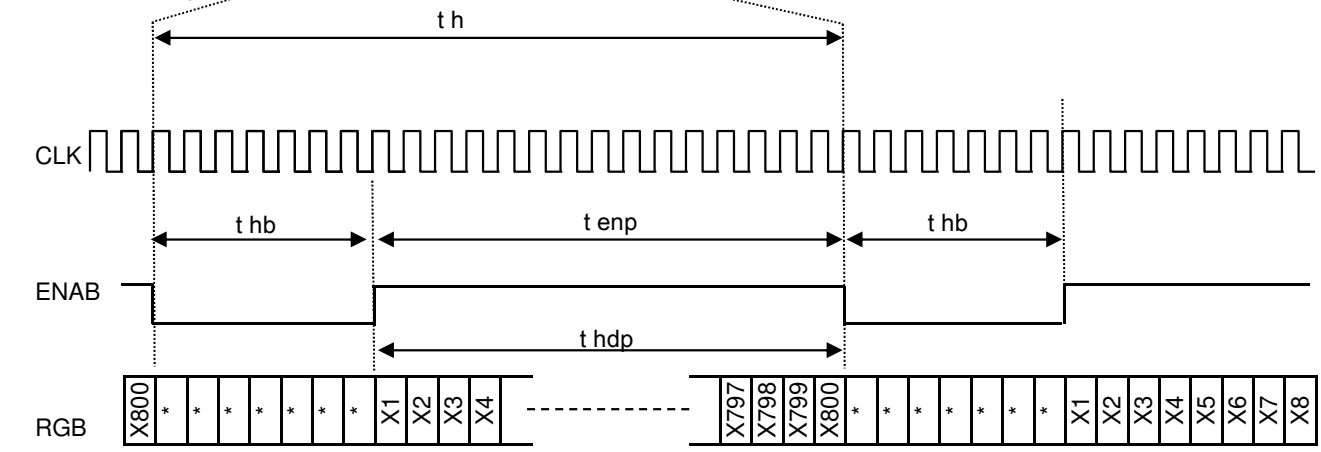
Item		Symbol	Rating			Unit	Signal (*)
			MIN	TYP	MAX		
CLK frequency		fCLK	(35)	40	(42)	MHz	CLK
Vertical	Frequency	fVD	(55)	60	(64.2)	Hz	VD,ENAB
	Period	tv	(613)	628	-	H	R[7:0],G[7:0],B[7:0]
	Blanking Time	tvb	(13)	28	-	H	
	Active Time	tvdp		600		H	
Horizontal	Frequency	fHD	(35.2)	37.9	(39.2)	kHz	CLK,HD,ENAB
	Period	th	(826)	1056	-	CLK	R[7:0],G[7:0],B[7:0]
	Blanking Time	thb	(26)	256	-	CLK	
	ENAB pulse width	tenp		800		CLK	
	Active Time	thdp		800		CLK	

(*) Input terminals are (R0 +/-, R1 +/-, R2 +/-, R3 +/-, CLK +/-).

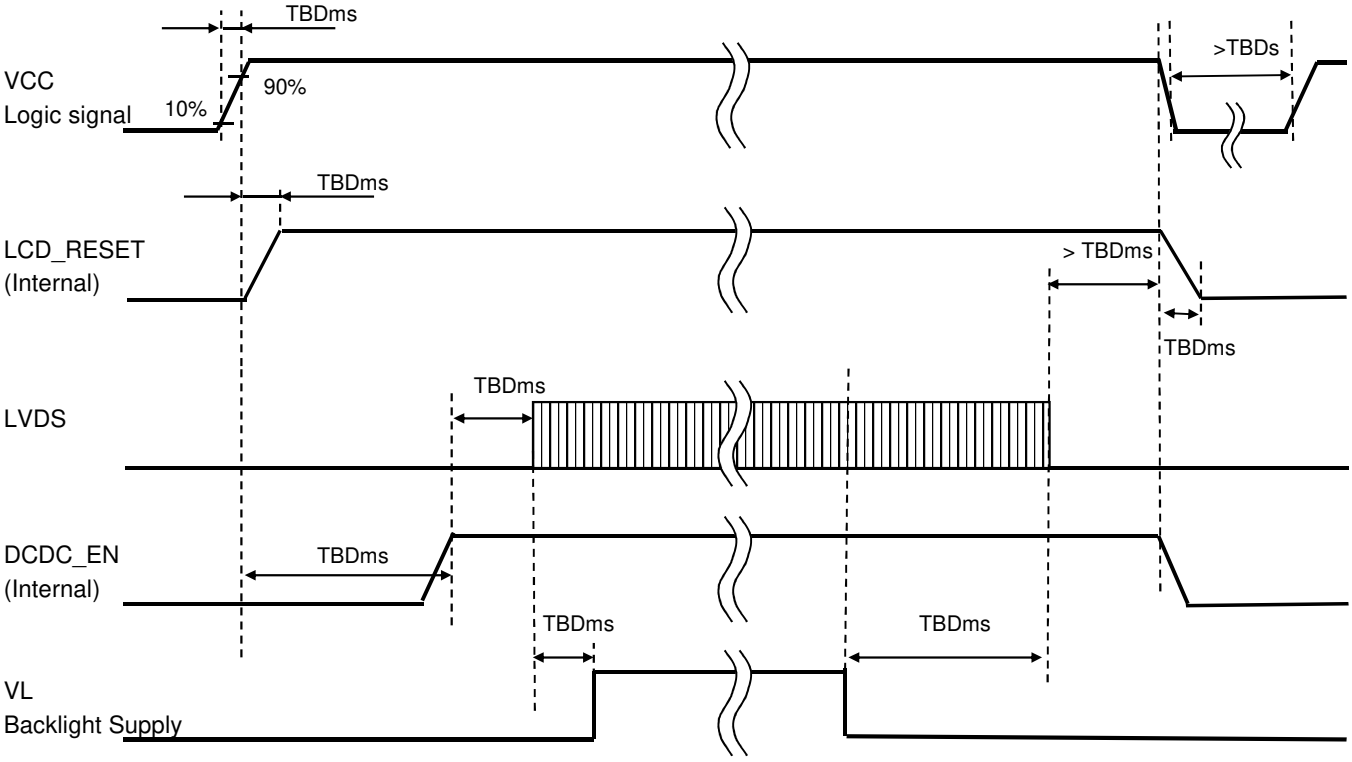
<Vertical timing>



<Horizontal timing>



6.4 Power ON/OFF Sequence



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