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Datasheet

LG Display

LP125WF4-SPQ1

HD-10-149

SPECIFICATION FOR APPROVAL

() Preliminary Specification

(◆) Final Specification

| | |
|-------|-------------------|
| Title | 12.5" FHD TFT LCD |
|-------|-------------------|

| | |
|----------|-------|
| Customer | |
| MODEL | DND8T |

| | |
|----------|----------------------|
| SUPPLIER | LG Display Co., Ltd. |
| *MODEL | LP125WF4 |
| Suffix | SPQ1 |

*When you obtain standard approval,
please use the above model name without suffix

| APPROVED BY | SIGNATURE |
|-------------|-----------|
| / | _____ |
| / | _____ |
| / | _____ |

| APPROVED BY | SIGNATURE |
|-----------------------|-----------|
| J. Y. Lee / Manager | _____ |
| REVIEWED BY | |
| Y. S. Ha / Manager | _____ |
| PREPARED BY | |
| H. G. Kim / Engineer | |
| S. H. Kang / Engineer | |
| K. H. Lee / Engineer | _____ |

Please return 1 copy for your confirmation with your signature and comments.

**Products Engineering Dept.
LG Display Co., Ltd**

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Product Specification

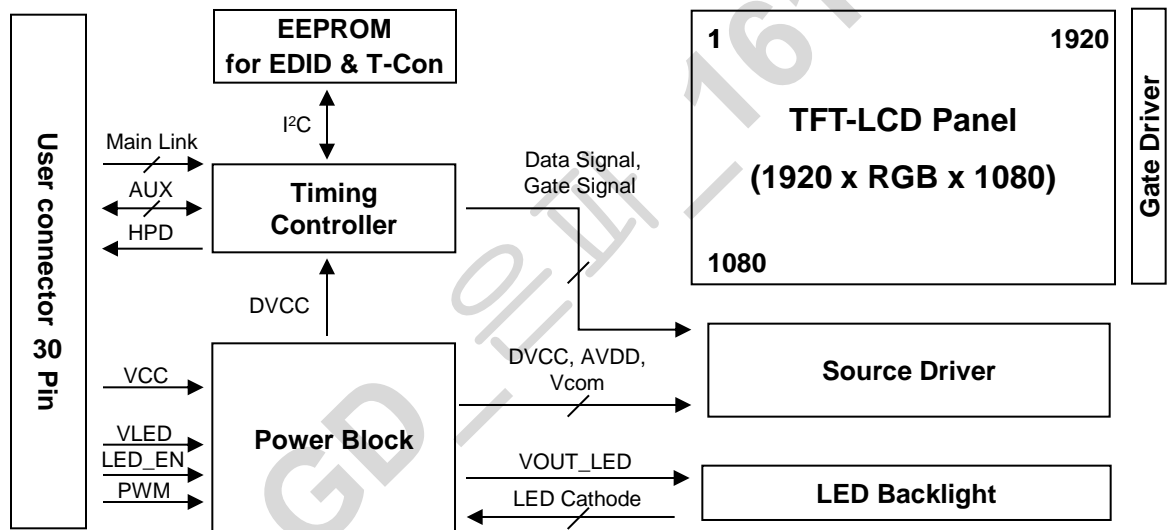
Record of Revisions

| Revision No | Revision Date | Page | Description | EDID version |
|-------------|---------------|-----------------------------|---|--------------|
| 0.0 | Mar. 10. 2016 | - | First Draft (Preliminary Specification) | 0.1 |
| 0.1 | Aug. 22. 2016 | 16, 17 26, 27 42 ~ 44 | Optical Specifications Update (Color Coordinate, Gray Scale) Packing Information Update EDID Update (Revision Code : A00) | 0.2 |
| 1.0 | Oct. 25. 2016 | | Final CAS Release | |
| | | 25~27 | Packing Information Update | |
| | | 21 | Drawing Update (Label Position) | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

LGD - 인포 - 161228

1. General Description

The LP125WF4 is a Color Active Matrix Liquid Crystal Display with an integral LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. This TFT-LCD has 12.5 inches diagonally measured active display area with HD resolution (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 6-bit gray scale signal for each dot, thus, presenting a palette of more than 262,144 colors. The LP125WF4 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP125WF4 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP125WF4 characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

| | |
|------------------------|---|
| Active Screen Size | 12.5 inches diagonal |
| Outline Dimension | 290.5(H, typ) × 170.7(V, typ) × 2.85(D,max) [mm] |
| Pixel Pitch | 0.144mm x 0.144mm (176ppi) |
| Pixel Format | 1920 horiz. By 1080 vert. Pixels RGB strip arrangement |
| Color Depth | 6-bit, 262,144 colors |
| Luminance, White | 300 cd/m ² |
| Power Consumption | Total 2.8 W(Typ.) Logic : 0.8 W (Typ.@ Mosaic), B/L : 2.00 W (Typ.@ VLED 12V) |
| Weight | 230g (Max.) |
| Display Operating Mode | Transmissive mode, normally black |
| Surface Treatment | Glare treatment of the front Polarizer (3H) |
| RoHS Compliance | Yes |
| BFR / PVC / As Free | Yes for all |

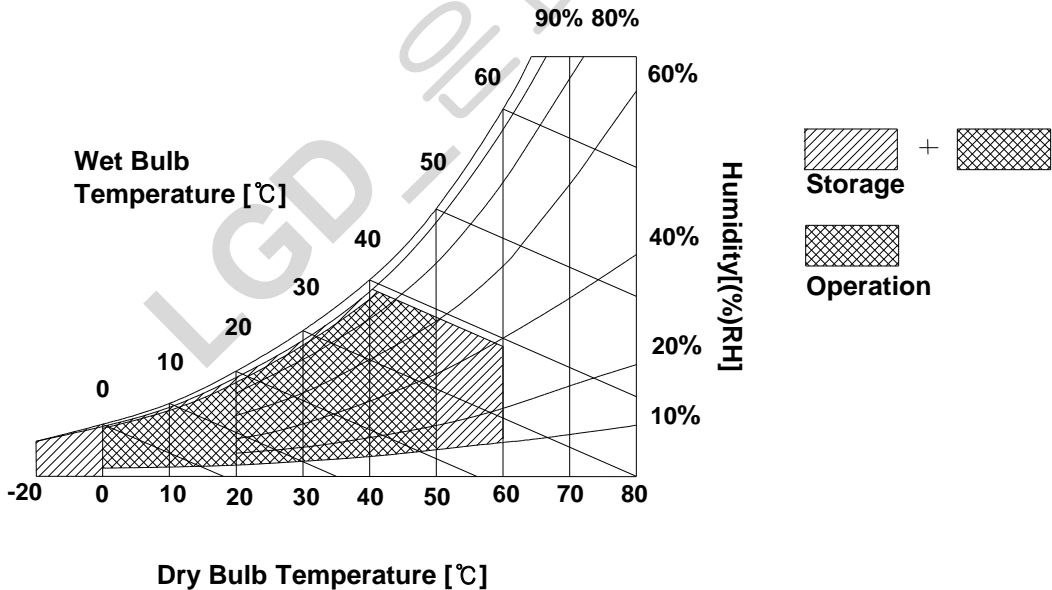
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Values | | Units | Notes |
|----------------------------|--------|--------|-----|-----------------|-------------|
| | | Min | Max | | |
| Power Input Voltage | VCC | -0.3 | 4.0 | V _{DC} | at 25 ± 2°C |
| Operating Temperature | TOP | 0 | 50 | °C | 1 |
| Storage Temperature | HST | -20 | 60 | °C | 1 |
| Operating Ambient Humidity | HOP | 10 | 90 | %RH | 1 |
| Storage Humidity | HST | 10 | 90 | %RH | 1 |

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.
Note : 2. Storage Condition is guaranteed under packing condition.



3. Electrical Specifications

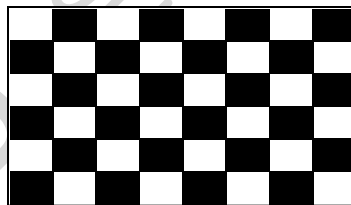
3-1. LCD Electrical Characteristics

Table 2. LCD ELECTRICAL CHARACTERISTICS

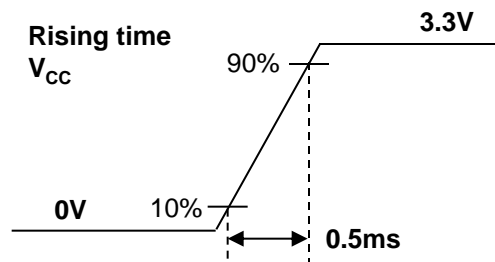
| Parameter | Symbol | Values | | | Unit | Notes |
|--------------------------------------|--------------------|--------|-----|-----|-------------------|-------|
| | | Min | Typ | Max | | |
| Power Supply Input Voltage | V_{CC} | 3.0 | 3.3 | 3.6 | V | 1 |
| Permissive Power Supply Input Ripple | V_{CCrp} | - | - | 100 | mV _{p-p} | |
| Power Supply Input Current | Mosaic I_{CC} | - | 242 | 273 | mA | 2 |
| Power Consumption | P_{CC} | - | 0.8 | 0.9 | W | |
| Power Supply Inrush Current | I_{CC_P} | - | - | 1.5 | A | 3 |
| Differential Impedance | Z_{LVDS} | 90 | 100 | 110 | Ω | |

Note)

- The measuring position is the connector of LCM and the test conditions are under 25°C, $f_v = 60\text{Hz}$
- The specified I_{CC} current and power consumption are under the $V_{CC} = 3.3\text{V}$, 25°C, $f_v = 60\text{Hz}$ condition and Mosaic pattern.



- The V_{CC} rising time is same as the minimum of T1 at Power on sequence.



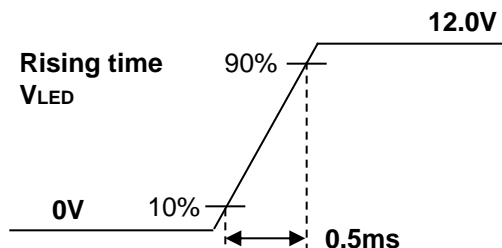
3-2. LED Backlight Electrical Characteristics

Table 3. LED B/L ELECTRICAL CHARACTERISTICS

| Parameter | | Symbol | Values | | | Unit | Notes |
|--------------------------|--------------------|------------------|--------|------|------|------|-------|
| | | | Min | Typ | Max | | |
| LED Power Input Voltage | | V_{LED} | 5.0 | 12.0 | 21.0 | V | 1 |
| LED Power Input Current | | I_{LED} | - | 167 | 175 | mA | 2 |
| LED Power Consumption | | P_{LED} | - | 2.0 | 2.1 | W | |
| LED Power Inrush Current | | I_{LED_P} | - | - | 1.5 | A | 3 |
| PWM Duty Ratio | | | 5 | - | 100 | % | 4 |
| PWM Jitter | | | 0 | - | 0.2 | % | 5 |
| PWM Frequency | | F_{PWM} | 200 | - | 1000 | Hz | 6 |
| PWM | High Level Voltage | V_{PWM_H} | 2.5 | - | 3.6 | V | |
| | Low Level Voltage | V_{PWM_L} | 0 | - | 0.3 | V | |
| LED_EN | High Voltage | $V_{LED_EN_H}$ | 2.5 | - | 3.6 | V | |
| | Low Voltage | $V_{LED_EN_L}$ | 0 | - | 0.3 | V | |
| Life Time | | | 15,000 | - | - | Hrs | 7 |

Note)

- The measuring position is the connector of LCM and the test conditions are under 25°C.
- The current and power consumption with LED Driver are under the $V_{LED} = 12.0V$, 25°C, PWM Duty 100% and White pattern with the normal frame frequency operated(60Hz).
- The V_{LED} rising time is same as the minimum of T13 at Power on sequence.

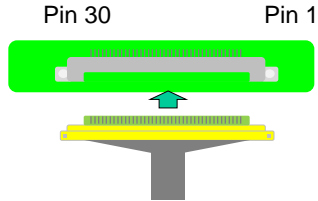


- The operation of LED Driver below minimum dimming ratio may cause flickering or reliability issue.
- If Jitter of PWM is bigger than maximum, it may induce flickering.
- This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz. In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
- The life time is determined as the time at which brightness of LCD is 50% compare to that of minimum value specified in table 7. under general user condition.

Product Specification

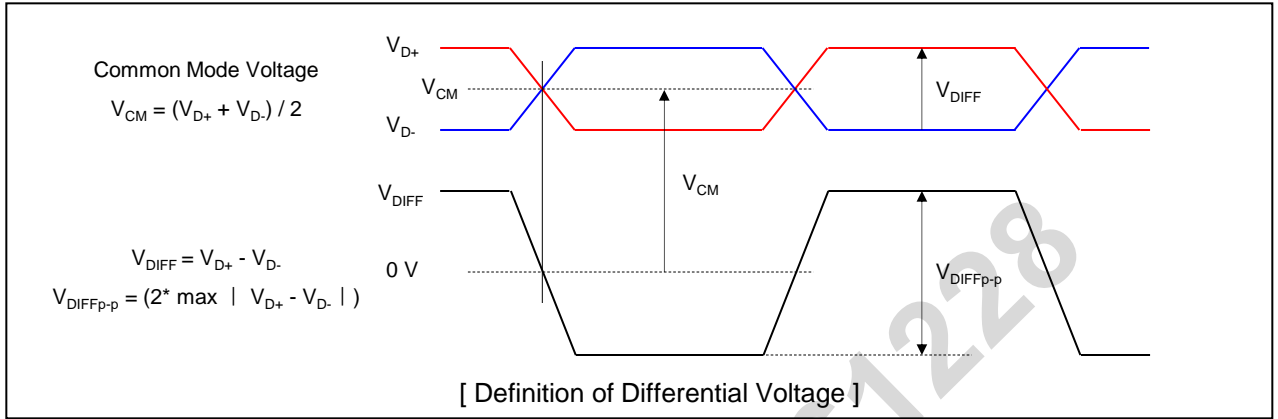
3-3. Interface Connections

Table 4. MODULE CONNECTOR PIN CONFIGURATION (CN1)

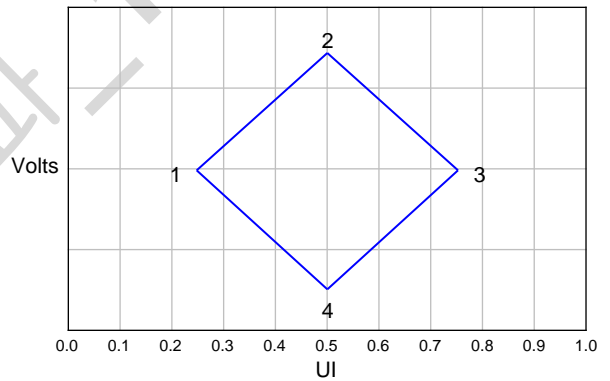
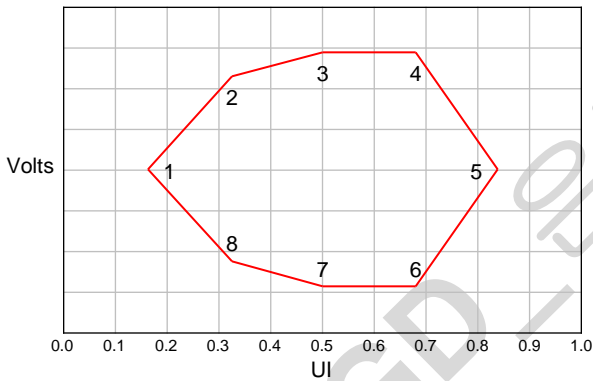
| Pin | Symbol | Description | Notes |
|-----|-------------|---|---|
| 1 | DBC_EN | DBC function (Active high). If to be disabled, should be tied to GND | [Connector] JAE, HD2S030HA1 or equivalent [Connector pin arrangement]  [LGD P-Vcom using information] 1. Pin for P-Vcom : #25, #30 2. P-Vcom Address : 0101000x |
| 2 | GND | High Speed Ground | |
| 3 | Lane1_N | Complement Signal Link Lane 1 | |
| 4 | Lane1_P | True Signal Link Lane 1 | |
| 5 | GND | High Speed Ground | |
| 6 | Lane0_N | Complement Signal Link Lane 0 | |
| 7 | Lane0_P | True Signal Link Lane 0 | |
| 8 | GND | High Speed Ground | |
| 9 | AUX_CH_P | True Signal Auxiliary Channel | |
| 10 | AUX_CH_N | Complement Signal Auxiliary Channel | |
| 11 | GND | High Speed Ground | |
| 12 | VCC | LCD logic and driver power | |
| 13 | VCC | LCD logic and driver power | |
| 14 | BIST | Built-In Self Test (active high) | |
| 15 | GND | LCD logic and driver ground | |
| 16 | GND | LCD logic and driver ground | |
| 17 | HPD | HPD signal pin | |
| 18 | BL_GND | LED Backlight ground | |
| 19 | BL_GND | LED Backlight ground | |
| 20 | BL_GND | LED Backlight ground | |
| 21 | BL_GND | LED Backlight ground | |
| 22 | BL ENABLE | LED Backlight control on/off control | |
| 23 | BL PWM | System PWM signal input for dimming | |
| 24 | HSO | H_sync for active touch | |
| 25 | NC Reserved | Reserved for LCD manufacture's use | |
| 26 | VLED | LED Backlight power (12V Typical) | |
| 27 | VLED | LED Backlight power (12V Typical) | |
| 28 | VLED | LED Backlight power (12V Typical) | |
| 29 | VLED | LED Backlight power (12V Typical) | |
| 30 | NC Reserved | Reserved for LCD manufacture's use | |

3-4. eDP Signal Timing Specifications

3-4-1. Definition of Differential Voltage



3-4-2. Main Link EYE Diagram



| Point | Reduced Bit Rate | | High Bit Rate | |
|-------|------------------|------------|---------------|------------|
| | Time(UI) | Voltage(V) | Time(UI) | Voltage(V) |
| 1 | 0.127 | 0.000 | 0.210 | 0.000 |
| 2 | 0.291 | 0.160 | 0.355 | 0.140 |
| 3 | 0.500 | 0.200 | 0.500 | 0.175 |
| 4 | 0.709 | 0.200 | 0.645 | 0.175 |
| 5 | 0.873 | 0.000 | 0.790 | 0.000 |
| 6 | 0.709 | -0.200 | 0.645 | -0.175 |
| 7 | 0.500 | -0.200 | 0.500 | -0.175 |
| 8 | 0.291 | -0.160 | 0.355 | -0.140 |

[EYE Mask Vertices at Source Connector Pins]

| Point | Reduced Bit Rate | | High Bit Rate | |
|-------|------------------|------------|---------------|------------|
| | Time(UI) | Voltage(V) | Time(UI) | Voltage(V) |
| 1 | 0.375 | 0.000 | 0.246 | 0.000 |
| 2 | 0.500 | 0.023 | 0.500 | 0.075 |
| 3 | 0.625 | 0.000 | 0.755 | 0.000 |
| 4 | 0.500 | -0.023 | 0.500 | -0.075 |

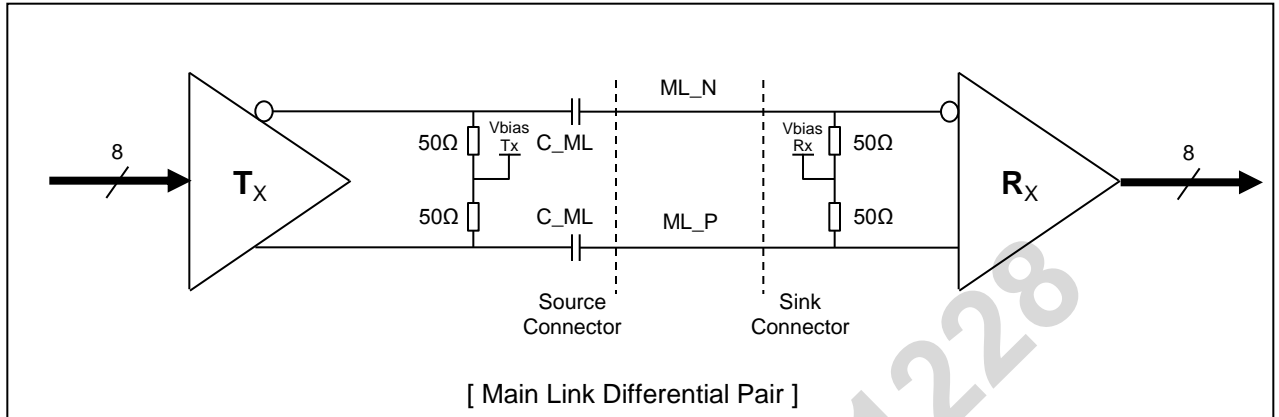
[EYE Mask Vertices at Sink Connector Pins]

| Point | Reduced Bit Rate | | High Bit Rate | |
|-------|------------------|------------|---------------|------------|
| | Time(UI) | Voltage(V) | Time(UI) | Voltage(V) |
| 1 | 0.270 | 0.000 | 0.246 | 0.000 |
| 2 | 0.500 | 0.068 | 0.500 | 0.075 |
| 3 | 0.731 | 0.000 | 0.755 | 0.000 |
| 4 | 0.500 | -0.068 | 0.500 | -0.075 |

[EYE Mask Vertices at embedded DP Sink Connector Pins]

Product Specification

3-4-3. eDP Main Link Signal

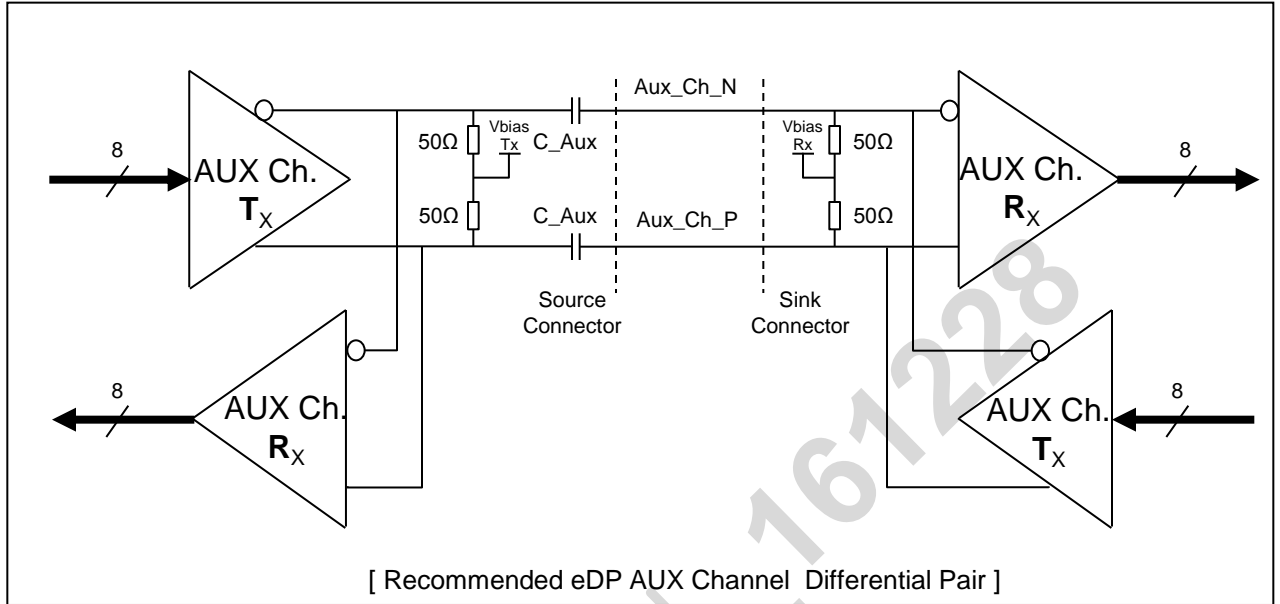


| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|-------------------|------|-----|-----|------|-------------------|
| Unit Interval for high bit rate (2.7Gbps / lane) | UI_HBR | - | 370 | - | ps | |
| Unit Interval for reduced bit rate (1.62Gbps / lane) | UI_RBR | - | 617 | - | ps | |
| Link Clock Down Spreading | Amplitude | 0 | - | 0.5 | % | |
| | Frequency | 30 | - | 33 | kHz | |
| Differential peak-to-peak voltage at Source side connector | $V_{TX-DIFFP-P}$ | 350 | - | - | mV | For HBR(2.7Gbps) |
| | | 400 | - | - | | For RBR(1.62Gbps) |
| EYE width at Source side connector | $T_{TX-EYE-CONN}$ | 0.58 | - | - | UI | For HBR(2.7Gbps) |
| | | 0.75 | - | - | UI | For RBR(1.62Gbps) |
| Differential peak-to-peak voltage at Sink side connector | $V_{RX-DIFFP-P}$ | 150 | - | - | mV | For HBR(2.7Gbps) |
| | | 136 | - | - | | For RBR(1.62Gbps) |
| EYE width at Sink side connector | $T_{RX-EYE-CONN}$ | 0.51 | - | - | UI | For HBR(2.7Gbps) |
| | | 0.46 | - | - | UI | For RBR(1.62Gbps) |
| Rx DC common mode voltage | $V_{RX CM}$ | 0 | - | 1.0 | V | |
| AC Coupling Capacitor | $C_{SOURCE-ML}$ | 75 | | 200 | nF | Source side |

Note)

1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. In cabled embedded system, it is recommended the system designer ensure that EYE width and voltage are met at the sink side connector pins.

3-4-4. eDP AUX Channel Signal

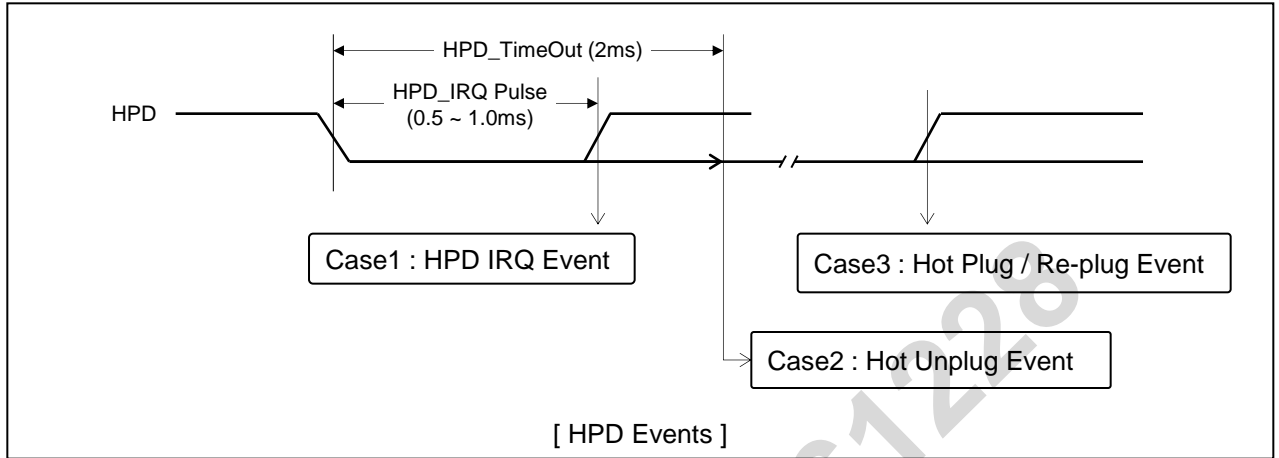


| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|-------------------|------|-----|------|------|---------------|
| AUX Unit Interval | UI | 0.4 | - | 0.6 | us | |
| AUX Jitter at Tx IC Package Pins | T_{jitter} | - | - | 0.04 | UI | Equal to 24ns |
| AUX Jitter at Rx IC Package Pins | | - | - | 0.05 | UI | Equal to 30ns |
| AUX Peak-to-peak voltage at Connector Pins of Receiving | $V_{AUX-DIFFp-p}$ | 0.39 | - | 1.38 | V | |
| AUX Peak-to-peak voltage at Connector Pins of Transmitting | | 0.36 | - | 1.36 | V | |
| AUX EYE width at Connector Pins of Tx and Rx | | 0.98 | - | - | UI | |
| AUX DC common mode voltage | V_{AUX-CM} | 0 | - | 1.0 | V | |
| AUX AC Coupling Capacitor | $C_{SOURCE-AUX}$ | 75 | | 200 | nF | Source side |

Note)

1. Termination resistor is typically integrated into the transmitter and receiver implementations.
2. AC Coupling Capacitor is not placed at the sink side.
3. $V_{AUX-DIFFp-p} = 2 * | V_{AUXP} - V_{AUXN} |$

3-4-5. eDP HPD Signal



| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--------------------------------|---------|------|-----|-----|------|-----------------------|
| HPD Voltage | HPD | 2.25 | - | 3.6 | V | Sink side Driving |
| Hot Plug Detection Threshold | | 2.0 | - | - | V | Source side Detecting |
| Hot Unplug Detection Threshold | | - | - | 0.8 | V | |
| HPD_IRQ Pulse Width | HPD_IRQ | 0.5 | - | 1.0 | ms | |
| HPD_TimeOut | | 2.0 | - | - | ms | HPD Unplug Event |

Note)

1. HPD IRQ : Sink device wants to notify the Source device that Sink's status has changed so it toggles HPD line, forcing the Source device to read its Link / Sink Receiver DPCD field via the AUX-CH
2. HPD Unplug : The Sink device is no longer attached to the Source device and the Source device may then disable its Main Link as a power saving mode
3. Plug / Re-plug : The Sink device is now attached to the Source device, forcing the Source device to read its Receiver capabilities and Link / Sink status Receiver DPCD fields via the AUX-CH

Product Specification

3-5. Signal Timing Specifications

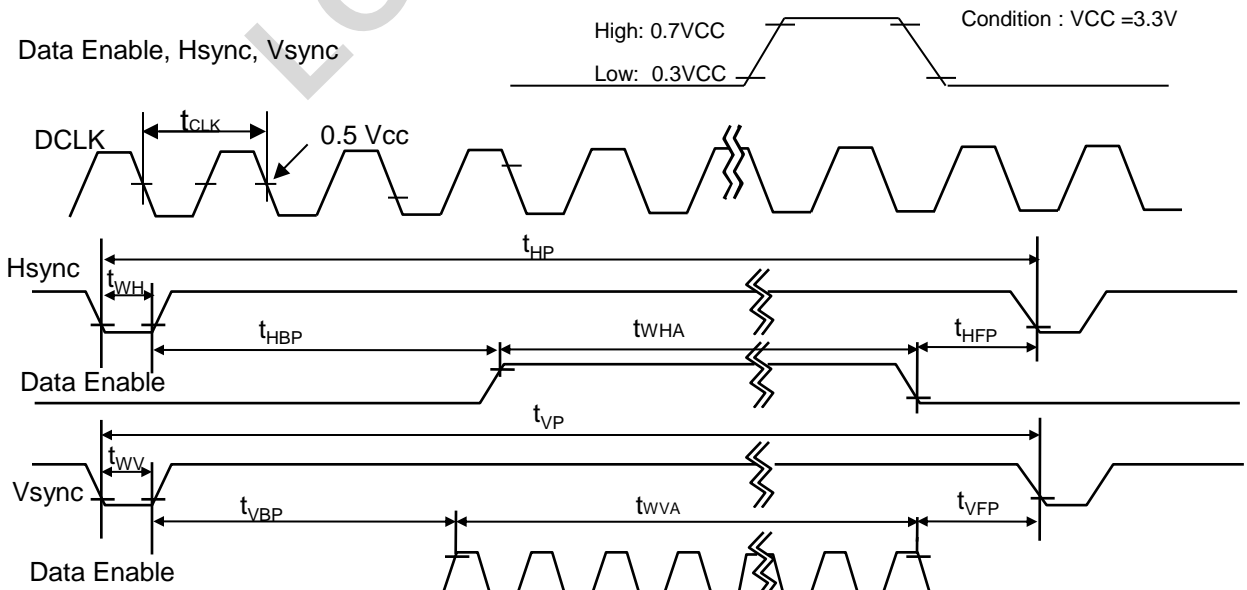
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of eDP Tx/Rx for its proper operation.

Table 4. TIMING TABLE

| ITEM | Symbol | Min | Typ | Max | Unit | Note |
|-------------|------------------------|-----------|------|-------|------|-----------|
| DCLK | Frequency | f_{CLK} | - | 138.7 | - | MHz |
| Hsync | Period | t_{HP} | 2068 | 2080 | 2092 | t_{CLK} |
| | Width | t_{WH} | 28 | 32 | 36 | |
| | Width-Active | t_{WHA} | 1920 | | | |
| Vsync | Period | t_{VP} | 1101 | 1111 | 1121 | t_{HP} |
| | Width | t_{WV} | 3 | 5 | 7 | |
| | Width-Active | t_{WVA} | 1080 | | | |
| Data Enable | Horizontal back porch | t_{HBP} | 76 | 80 | 84 | t_{CLK} |
| | Horizontal front porch | t_{HFP} | 44 | 48 | 52 | |
| | Vertical back porch | t_{VBP} | 16 | 23 | 30 | t_{HP} |
| | Vertical front porch | t_{VFP} | 2 | 3 | 4 | |

Notice. all reliabilities are specified for timing specification based on refresh rate of 60Hz. However, LP125WF4 has a good actual performance even at lower refresh rate (e.g. 40Hz or 50Hz) for power saving Mode, whereas LP125WF4 is secured only for function under lower refresh rate. 60Hz at Normal mode, 50Hz, 40Hz at Power save mode. Don't care Flicker level (Power save mode).

3-6. Signal Timing Waveforms



Product Specification

3-7. Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 5. COLOR DATA REFERENCE

| Color | | Input Color Data | | | | | | | | | | | | | | | | | | | |
|-------------|------------|------------------|----|----|----|----|----|-------|----|-----|----|----|----|------|----|-----|----|-----|----|--|--|
| | | RED | | | | | | GREEN | | | | | | BLUE | | | | | | | |
| | | MSB | | | | | | LSB | | MSB | | | | | | LSB | | MSB | | | |
| | | R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| Basic Color | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | |
| | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | |
| | Magenta | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | |
| | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | | |
| RED | RED (00) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | RED (01) | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | ... | ... | | | | | | ... | | | | | | ... | | | | | | | |
| | RED (62) | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | RED (63) | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| GREEN | GREEN (00) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | GREEN (01) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | ... | ... | | | | | | ... | | | | | | ... | | | | | | | |
| | GREEN (62) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | GREEN (63) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| BLUE | BLUE (00) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| | BLUE (01) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |
| | ... | ... | | | | | | ... | | | | | | ... | | | | | | | |
| | BLUE (62) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | | |
| | BLUE (63) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | | |

Product Specification

3-8. Power Sequence

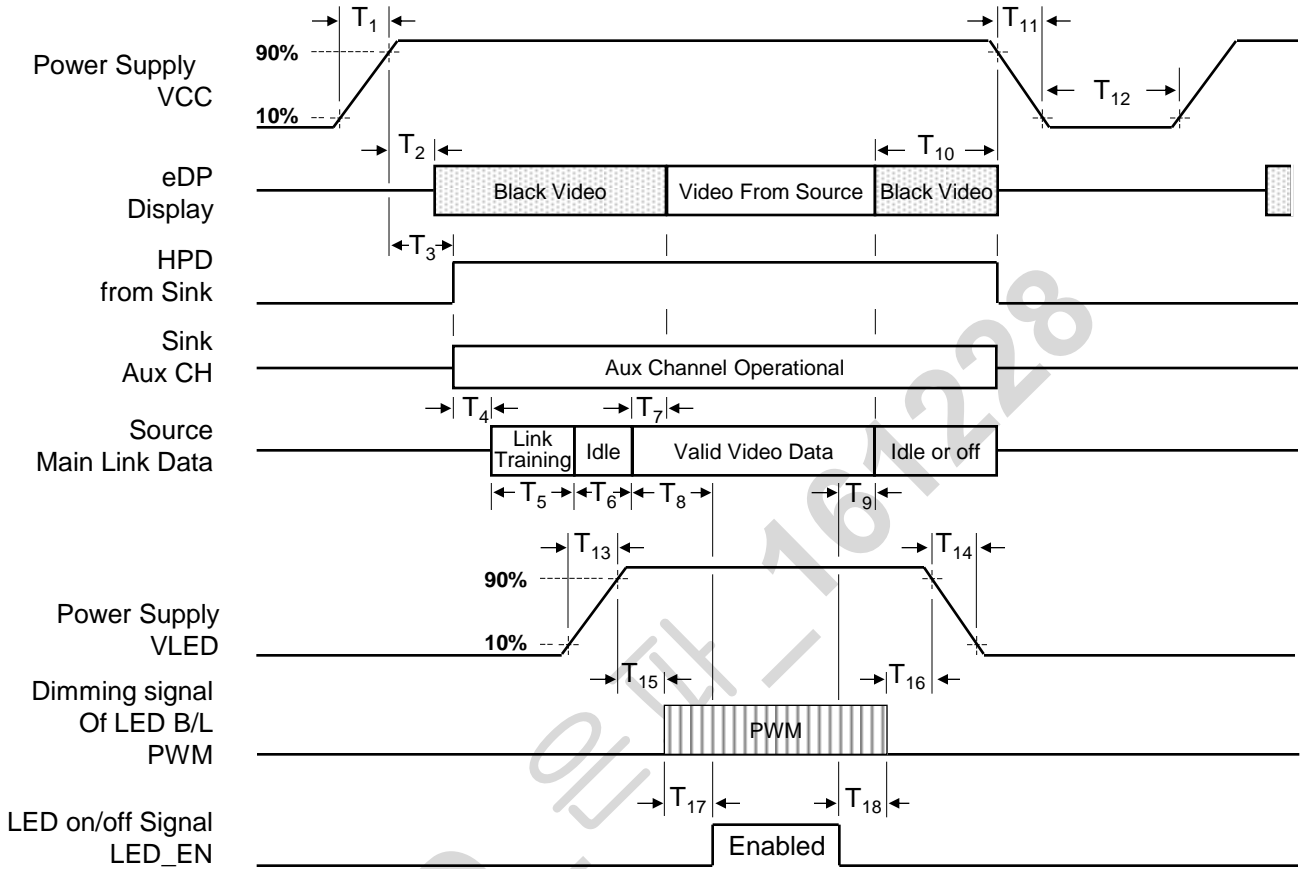


Table 6. POWER SEQUENCE TABLE

| Symbol | Required By | Limits | | Units | Notes | Symbol | Required By | Limits | | Units | Notes |
|----------------|-------------|--------|-----|-------|----------------------------|-----------------|-------------|--------|-----|-------|-------|
| | | Min | Max | | | | | Min | Max | | |
| T ₁ | Source | 0.5 | 10 | ms | - | T ₁₀ | Source | 0 | 500 | ms | - |
| T ₂ | Sink | 0 | 200 | ms | - | T ₁₁ | Source | - | 10 | ms | - |
| T ₃ | Sink | 0 | 200 | ms | - | T ₁₂ | Source | 500 | - | ms | - |
| T ₄ | Source | - | - | ms | - | T ₁₃ | Source | 0.5 | 10 | ms | - |
| T ₅ | Source | - | - | ms | - | T ₁₄ | Source | 0.5 | 10 | ms | - |
| T ₆ | Source | - | - | ms | - | T ₁₅ | Source | 10 | - | ms | - |
| T ₇ | Sink | 0 | 50 | ms | - | T ₁₆ | Source | 10 | - | ms | - |
| T ₈ | Source | - | - | ms | LGD recommend Min 200ms | T ₁₇ | Source | 0 | - | ms | - |
| T ₉ | Source | - | - | ms | - | T ₁₈ | Source | 0 | - | ms | - |

- Note) 1. Do not insert the mating cable when system turn on.
 2. Valid Data have to meet "3-3. eDP Signal Timing Specifications"
 3. Video Signal, LED_EN and PWM need to be on pull-down condition on invalid status.
 4. LGD recommend the rising sequence of VLED after the Vcc and valid status of Video Signal turn on.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 20 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.

FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

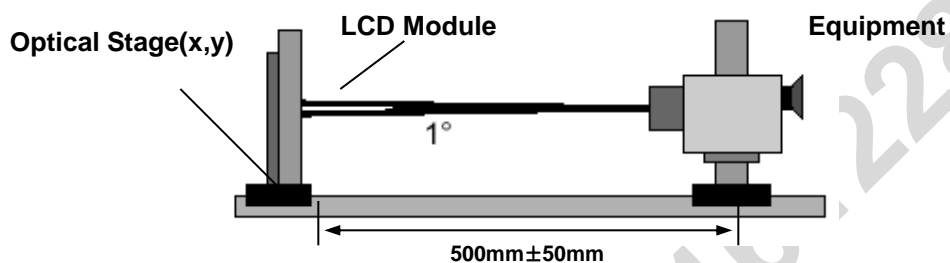


Table 7. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz

| Parameter | | Symbol | Values | | | Units | Notes |
|--------------------------|-----------------------------------|------------------------------|-------------------|-------|-------------------|-------------------|-------|
| | | | Min | Typ | Max | | |
| Contrast Ratio | | CR | 600 | 700 | - | | 1 |
| Surface Luminance, white | | L _{WH} | 255 | 300 | - | cd/m ² | 2 |
| Luminance Variation | | $\delta_{\text{WHITE}(5P)}$ | - | 1.2 | 1.4 | - | 3 |
| | | $\delta_{\text{WHITE}(13P)}$ | - | 1.4 | 1.6 | | |
| Response Time | | Tr + Tf | - | 25 | 35 | ms | 4 |
| Color Coordinates | RED | Rx | Typical - 0.03 | 0.589 | Typical + 0.03 | | |
| | | Ry | | 0.356 | | | |
| | GREEN | Gx | | 0.335 | | | |
| | | Gy | | 0.565 | | | |
| | BLUE | Bx | | 0.156 | | | |
| | | By | | 0.104 | | | |
| | WHITE | Wx | | 0.313 | | | |
| Wy | | 0.329 | | | | | |
| Viewing Angle | x axis, right ($\Phi=0^\circ$) | Θ_r | 80 | - | - | Degree | 5 |
| | x axis, left ($\Phi=180^\circ$) | Θ_l | 80 | - | - | | |
| | y axis, up ($\Phi=90^\circ$) | Θ_u | 80 | - | - | | |
| | y axis, down ($\Phi=270^\circ$) | Θ_d | 80 | - | - | | |
| Gray Scale | | | | | | | 6 |

Product Specification

Note)

1. It should be measured in the center of screen(1 Point). Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio(1 Point)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the average of 5 point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see FIG 2.

$$L_{WH} = \text{Average}(1,2, \dots 5 \text{ Point})$$

3. The variation in surface luminance , The panel total variation (δ WHITE) is determined by measuring N at each test position 1 through 13 and then defined as following numerical formula.
For more information see FIG 2.

$$\delta \text{ WHITE (5P)} = \frac{\text{Maximum (1,2, \dots 5 Point)}}{\text{Minimum (1,2, \dots 5 Point)}} \quad \delta \text{ WHITE (13P)} = \frac{\text{Maximum (1,2, \dots 13 Point)}}{\text{Minimum (1,2, \dots 13 Point)}}$$

4. Response time is the time required for the display to transition from black to white (rise time, T_r) and from white to black (falling time, T_f). For additional information see FIG 3.
5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.
6. Gray scale specification

| Gray Level | Luminance [%] (Typ) |
|------------|---------------------|
| L0 | 0.16 |
| L7 | 0.97 |
| L15 | 4.26 |
| L23 | 10.5 |
| L31 | 19.8 |
| L39 | 33.6 |
| L47 | 52.1 |
| L55 | 74.8 |
| L63 | 100 |

FIG. 2 Luminance

<Measuring point for Average Luminance & measuring point for Luminance variation>

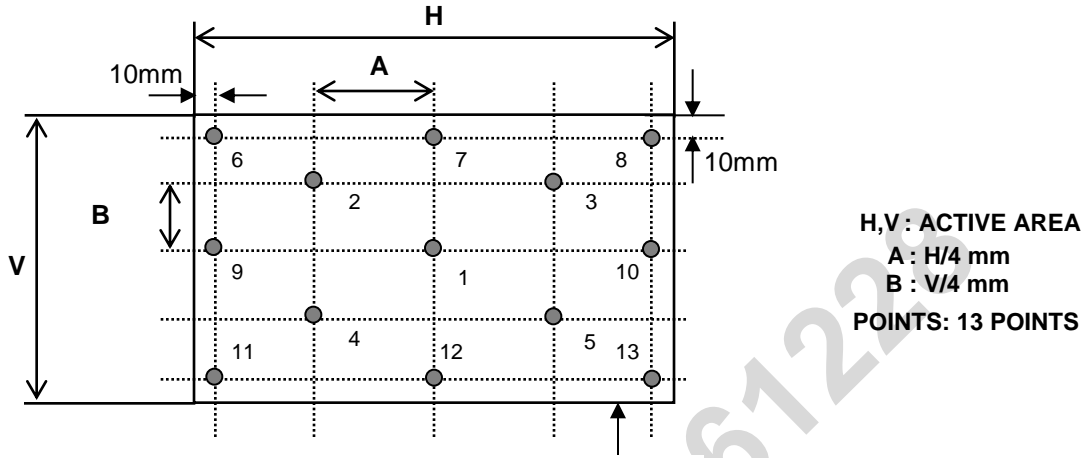


FIG. 3 Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".

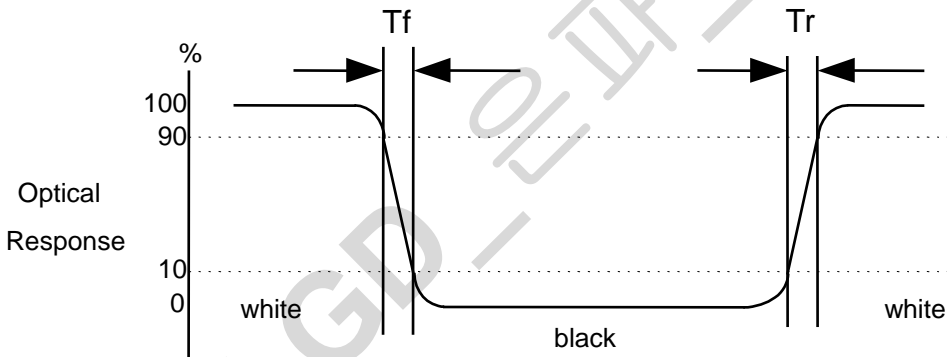
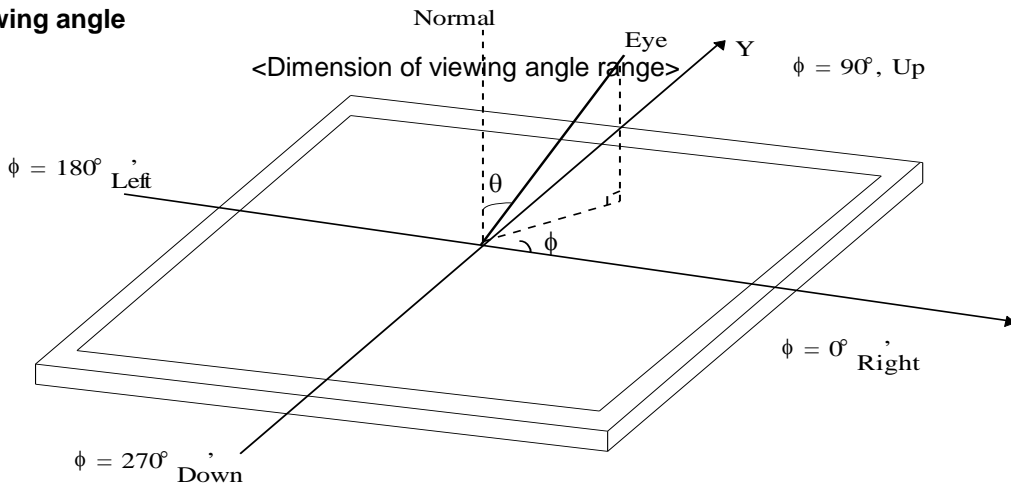


FIG. 4 Viewing angle



Product Specification

5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP125WF4. In addition the figures in the next page are detailed mechanical drawing of the LCD.

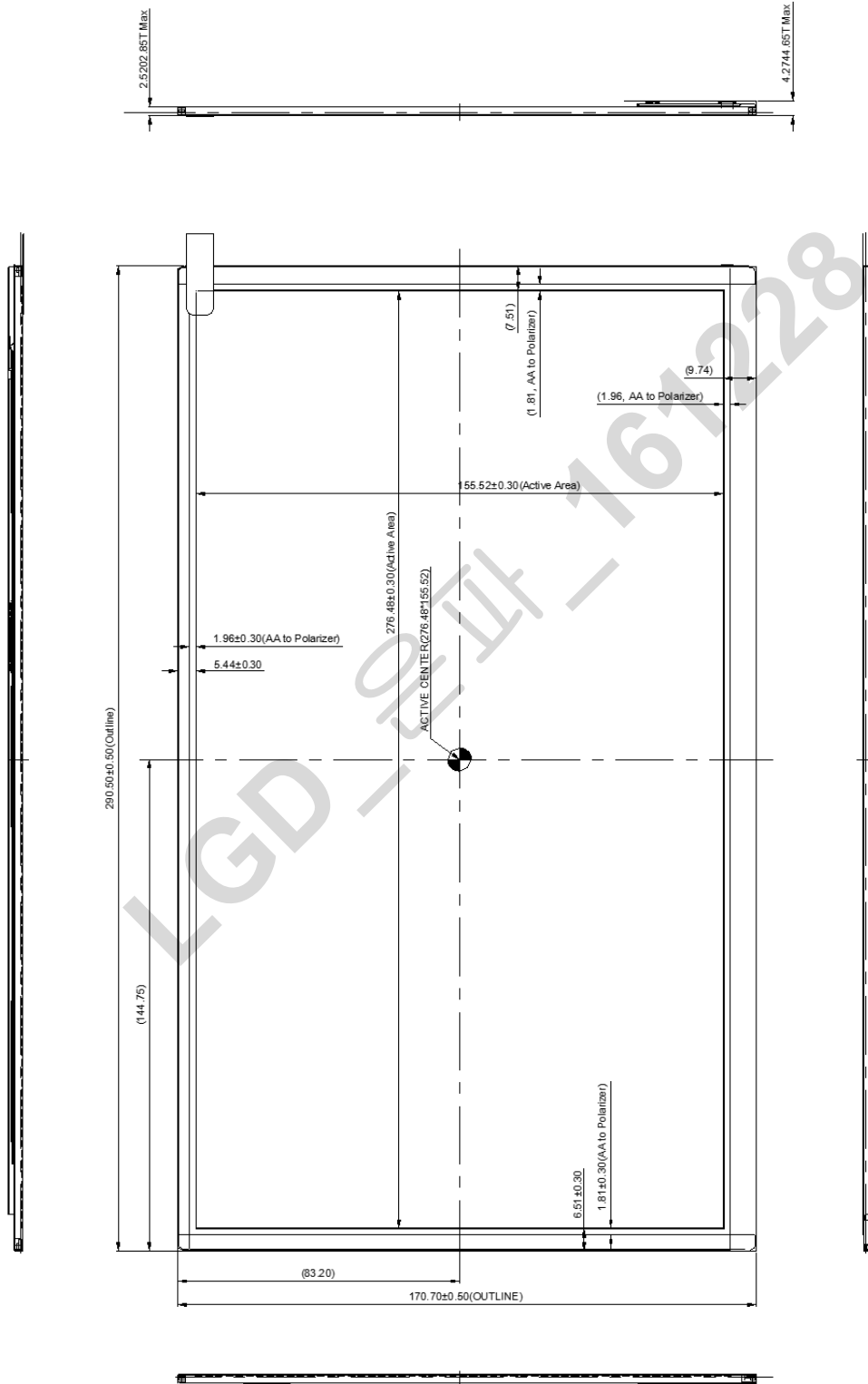
| | | |
|----------------------------|--|----------------|
| Outline Dimension | Horizontal | 290.5 ± 0.5mm |
| | Vertical | 170.7 ± 0.5mm |
| | Thickness | 2.85mm (max) |
| Active Display Area | Horizontal | 276.48 ± 0.5m |
| | Vertical | 155.52 ± 0.5mm |
| Weight | 230g (Max.) | |
| Surface Treatment | Glare treatment of the front polarizer | |

LGD - 인포 - 161218

Product Specification

<FRONT VIEW>

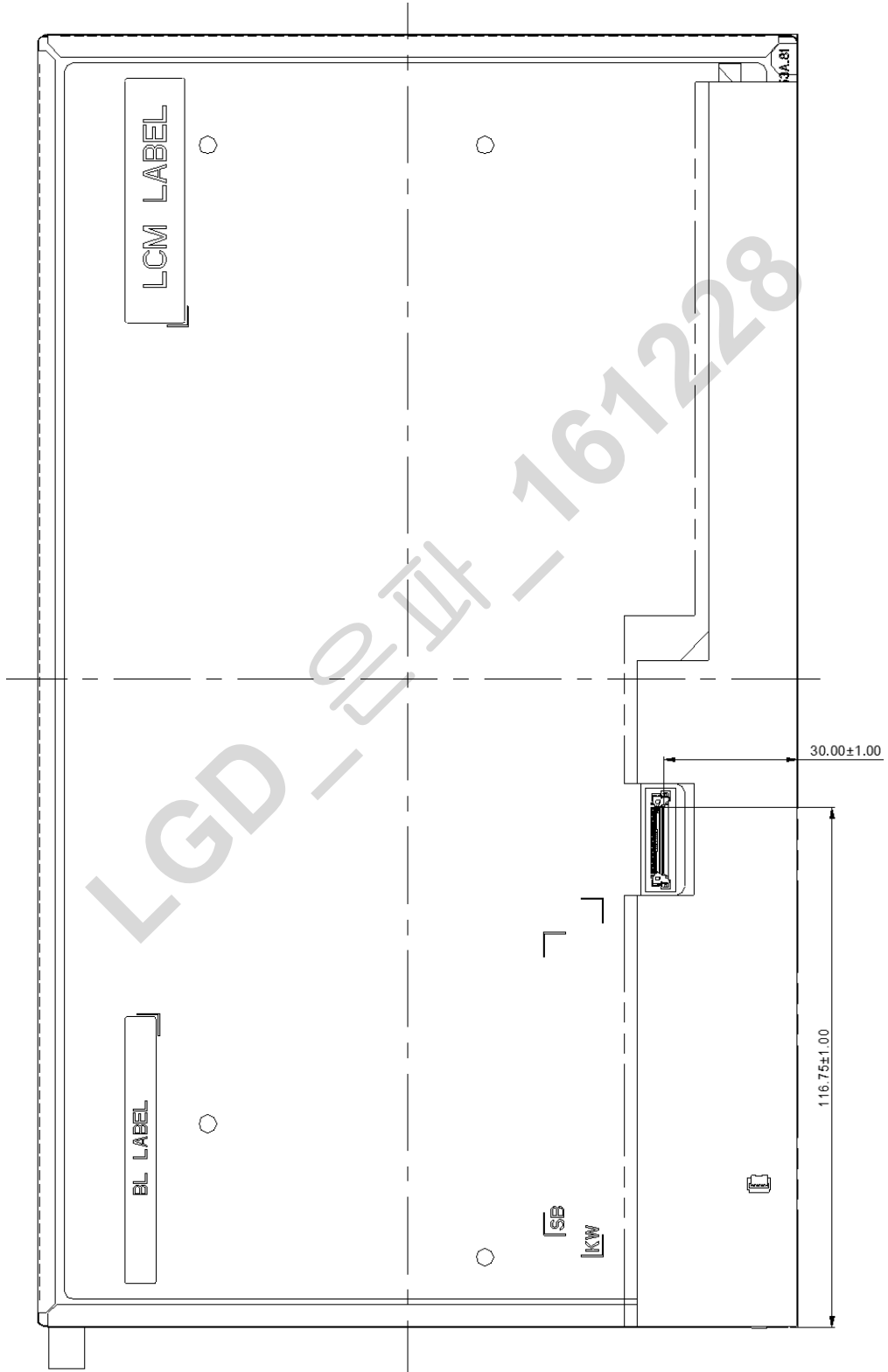
Note) Unit:[mm], General tolerance: $\pm 0.5\text{mm}$



Product Specification

<REAR VIEW>

Note) Unit:[mm], General tolerance: $\pm 0.5\text{mm}$



Product Specification

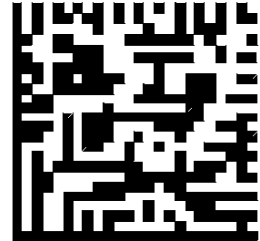
[**DETAIL INFORMATION OF PPID LABEL AND REVISION CODE**]

* Country of Origin

* PPID Label Revision

XX-0DND8T-56252-XXX-XXXX-XXX

D/PN : 0DND8T 12.5" FHD
LP125WF4 (SP)(Q1)



XXXXXXXXXXXXXXXX XXXX



* PPID Label Revision :

It is subject to change with Dell event. Please refer to the below table for detail.

| Classification | No Change | 1st Revision | 2nd Revision | ... | 9th Revision | ... |
|----------------|-----------|--------------|--------------|-----|--------------|-----|
| SST(WS) | X00 | X01 | X02 | ... | X09 | ... |
| PT(ES) | X10 | X11 | X12 | ... | X19 | ... |
| ST(CS) | X20 | X21 | X22 | ... | X29 | ... |
| XB(MP) | A00 | A01 | A02 | ... | A09 | ... |

| Country of Origin | Factory ID |
|-------------------|------------|
| CN: China | LGDNJ |
| KR: Korea | - |

Product Specification

6. Reliability

Environment test condition

| No. | Test Item | Conditions |
|-----|---------------------------------|---|
| 1 | High temperature storage test | Ta= 60°C, 240h |
| 2 | Low temperature storage test | Ta= -20°C, 240h |
| 3 | High temperature operation test | Ta= 50°C, 50%RH, 240h |
| 4 | Low temperature operation test | Ta= 0°C, 240h |
| 5 | Vibration test (non-operating) | Random, 1.0Grms, 10 ~ 300Hz(PSD 0.0035) 3 axis, 30min/axis |
| 6 | Shock test (non-operating) | - No functional or cosmetic defects following a shock to all 6 sides delivering at least 180 G in a half sine pulse no longer than 2 ms to the display module - No functional defects following a shock delivering at least 200 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays |
| 7 | Altitude | operating storage / shipment |
| | | 0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr |

{ Result Evaluation Criteria }

There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

In the Reliability Test, Confirm performance after leaving in room temp.

In the standard condition, there shall be no practical problems that may affect the display function 24 hours later after reliability test. After the reliability test, we can guarantee the product only when the corrosion is causing its malfunction. The corrosion causing no functional defect can not be guaranteed.

7. International Standards

7-1. Safety

- a) UL 60950-1, Underwriters Laboratories Inc.
Information Technology Equipment - Safety - Part 1 : General Requirements.
- b) CAN/CSA-C22.2 No. 60950-1-07, Canadian Standards Association.
Information Technology Equipment - Safety - Part 1 : General Requirements.
- c) EN 60950-1, European Committee for Electro technical Standardization (CENELEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.
- d) IEC 60950-1, The International Electro technical Commission (IEC).
Information Technology Equipment - Safety - Part 1 : General Requirements

7-2. Environment

- a) RoHS, Directive 2011/65/EU of the European Parliament and of the council of 8 June 2011

Product Specification

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | E | F | G | H | I | J | K | L | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|

A,B,C : SIZE(INCH)
 E : MONTH

D : YEAR
 F ~ M : SERIAL NO.

Note

1. YEAR

| | | | | | | | | | | |
|------|------|------|------|------|------|------|------|------|------|------|
| Year | 2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 |
| Mark | A | B | C | D | E | F | G | H | J | K |

2. MONTH

| | | | | | | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sep | Oct | Nov | Dec |
| Mark | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C |

b) Location of Lot Mark

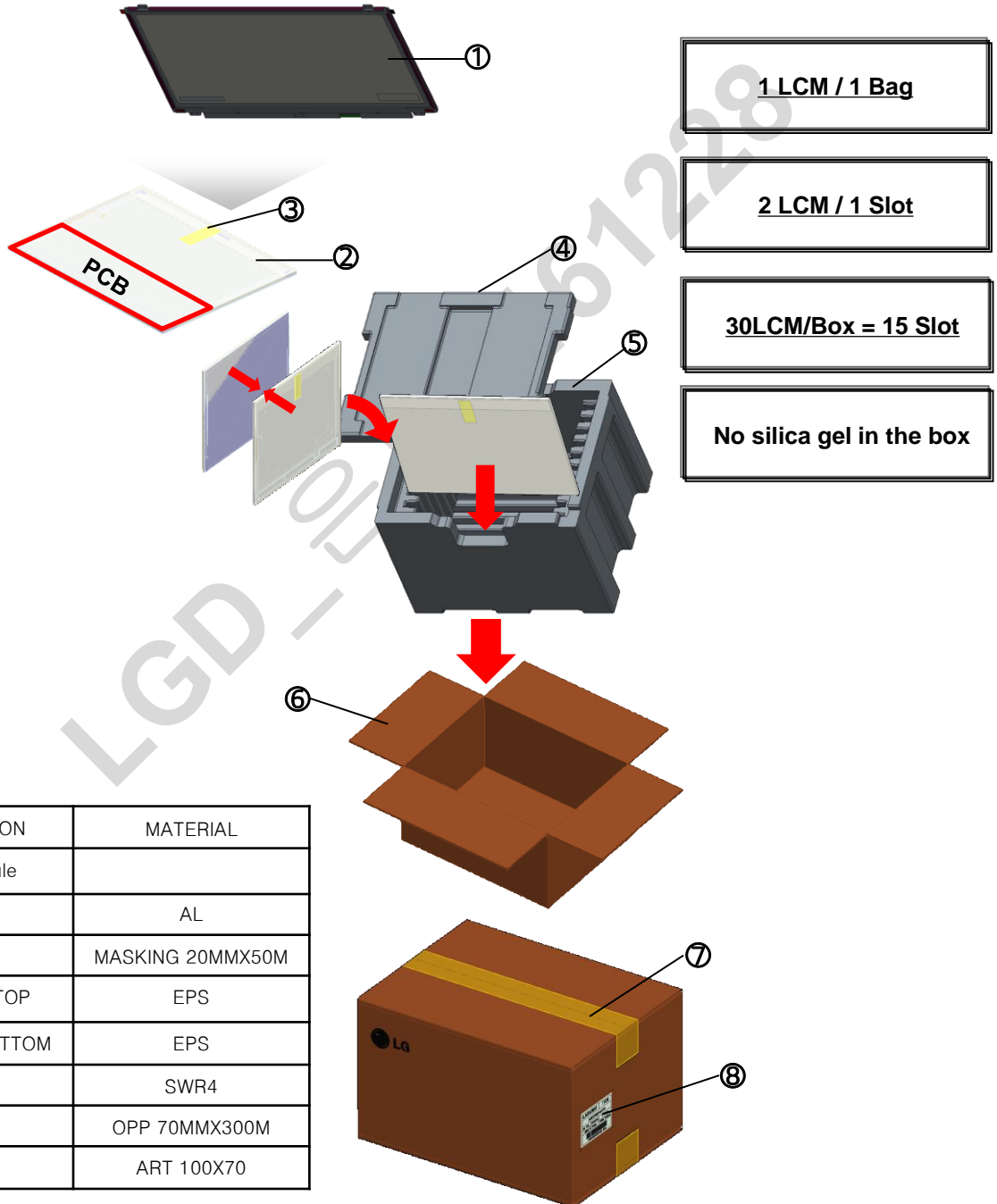
Serial No. is printed on the label. The label is attached to the backside of the LCD module.
 This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 30 pcs

b) Box Size : 478mm X 365mm X 244mm

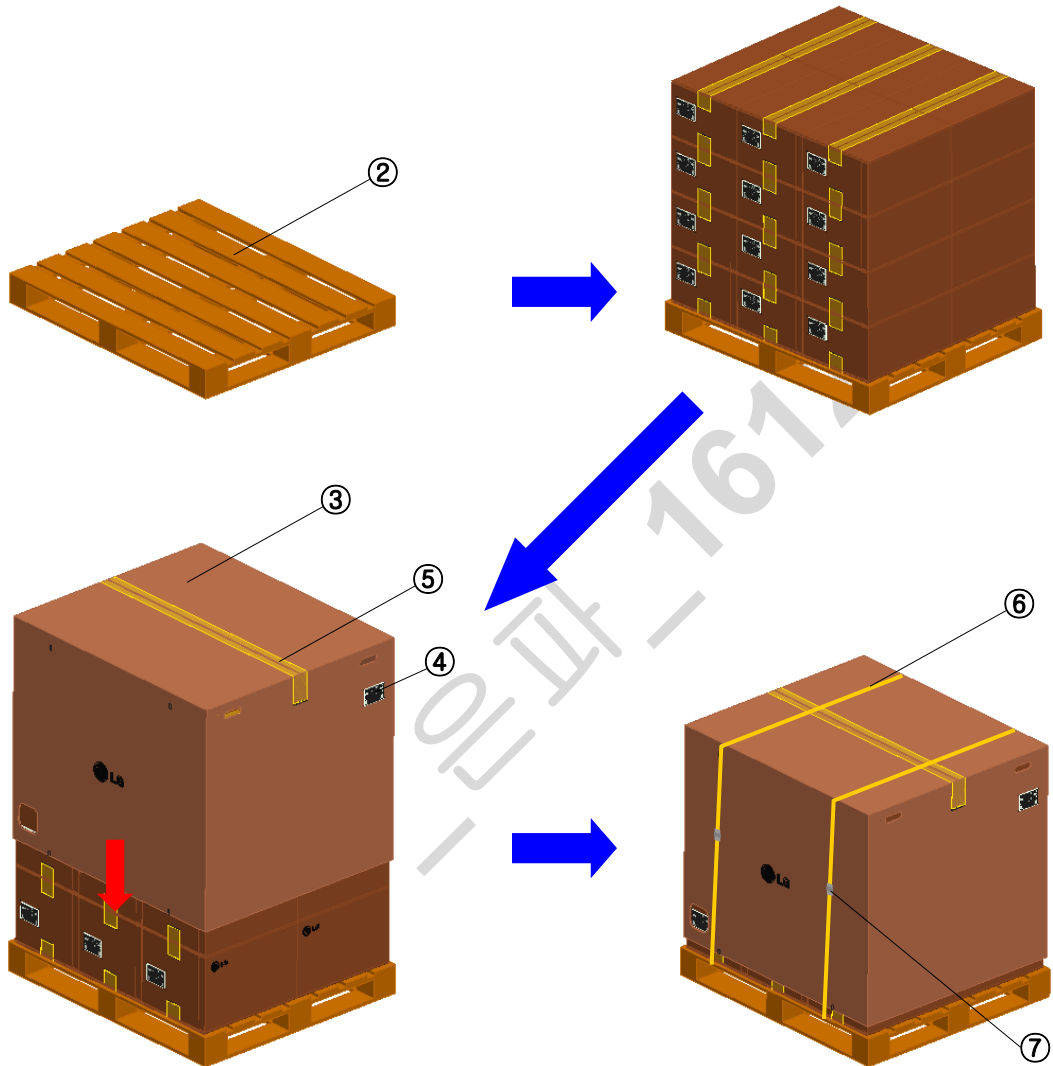
8-3. Packing Assembly



| NO. | DESCRIPTION | MATERIAL |
|-----|-----------------|------------------|
| 1 | LCD Module | |
| 2 | BAG | AL |
| 3 | TAPE | MASKING 20MMX50M |
| 4 | PACKING, TOP | EPS |
| 5 | PACKING, BOTTOM | EPS |
| 6 | BOX | SWR4 |
| 7 | TAPE | OPP 70MMX300M |
| 8 | LABEL | ART 100X70 |

<20LCM / Box>

8-4 Pallet Assembly



| NO. | DESCRIPTION | MATERIAL |
|-----|--------------|---------------|
| 1 | Packing AssY | |
| 2 | Pallet | Plywood |
| 3 | Angle Cover | SW |
| 4 | Label | YUPO 100X70 |
| 5 | TAPE | OPP 70MMX300M |
| 6 | Band | PP |
| 7 | CLIP | Steel |

9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to resist external force.
- (4) You should adopt radiation structure to satisfy the temperature specification.
- (5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- (6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
- (7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- (8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (9) Do not open the case because inside circuits do not have sufficient strength.
- (10) When handling the LCD module, it needs to handle with care not to give mechanical stress to the PCB and Mounting Hole area.”

9-2. OPERATING PRECAUTIONS

- (1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
 $V = \pm 200\text{mV}$ (Over and under shoot voltage)
- (2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
- (3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- (4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- (5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
- (6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

- (1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

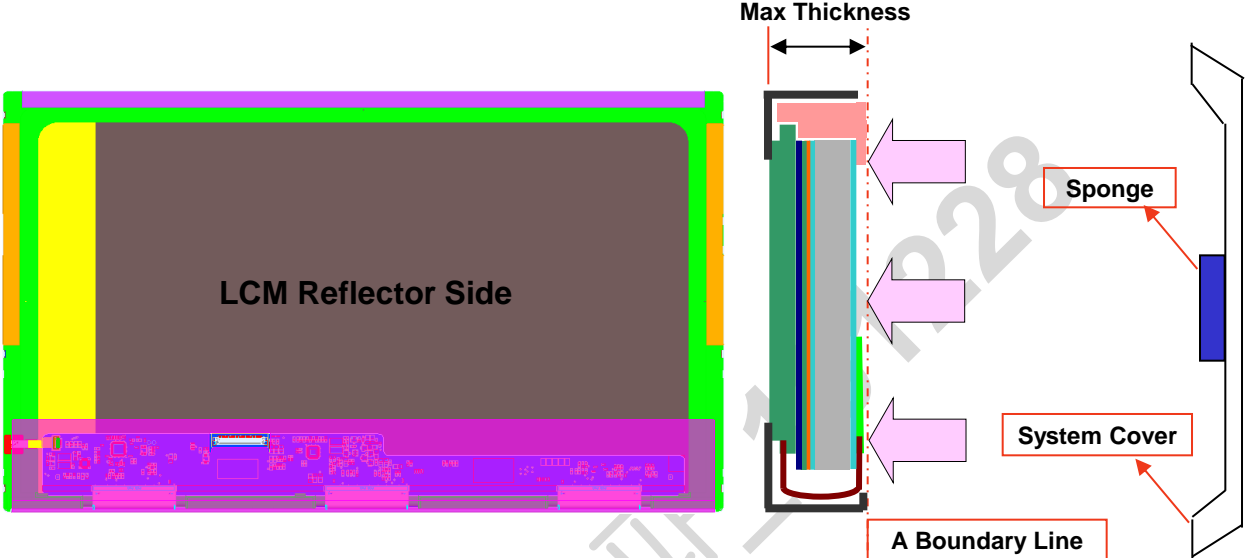
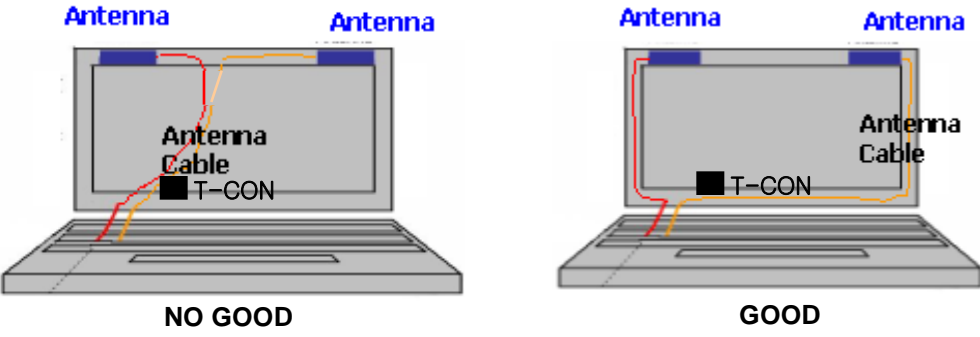
9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

- (1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- (2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
- (3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- (4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

9-7. THE LGD QA RESPONSIBILITY WILL BE AVOIDED IN CASE OF BELOW

- (1) When the customer attaches TSM(Touch Sensor Module) on LCM without Supplier's approval.
- (2) When the customer attaches cover glass on LCM without Supplier's approval.
- (3) When the LCMs were repaired by 3rd party without Supplier's approval.
- (4) When the LCMs were treated like Disassemble and Rework by the Customer and/or Customer's representatives without supplier's approval.

APPENDIX A. LGD Proposal for system cover design

| | |
|--|--|
| 1 | Gap check for securing the enough gap between LCM and System cover. |
|  <p>The diagram illustrates the assembly of the LCM (Liquid Crystal Module) and the system cover. On the left, a top-down view of the LCM reflector side is shown with various colored regions (yellow, green, orange, purple). On the right, a cross-sectional view shows the LCM, a boundary line, a sponge, and the system cover. A double-headed arrow indicates the 'Max Thickness' of the LCM. Labels include 'LCM Reflector Side', 'Max Thickness', 'Sponge', 'System Cover', and 'A Boundary Line'.</p> | |
| Define | <p>1. Rear side of LCM is sensitive against external stress, and previous check about interference is highly needed.</p> <p>2. In case there is something from system cover comes into the boundary above, mechanical interference may cause the FOS defects. (e.g.. Ripple, White spot..)</p> |
| 2 | Check if antenna cable is sufficiently apart from T-CON of LCD Module. |
|  <p>The diagrams show two scenarios for antenna cable placement relative to the T-CON (Thin-Film Transistor Driver) on the LCD module. The left diagram, labeled 'NO GOOD', shows the antenna cable overlapping the T-CON. The right diagram, labeled 'GOOD', shows the antenna cable separated from the T-CON. Labels include 'Antenna', 'Antenna Cable', and 'T-CON'.</p> | |
| Define | If system antenna is overlapped with T-CON, it might be cause the noise. |

APPENDIX A. LGD Proposal for system cover design

| | |
|--------|--|
| 3 | Gap check for securing the enough gap between LCM and System hinge. |
| | |
| Define | <ol style="list-style-type: none"> At least 2.0mm of gap needs to be secured to prevent the shock related defects. "L" type of hinge is recommended than "I" type under shock test. |
| 4 | Checking the path of the System wire. |
| | |
| Define | <ol style="list-style-type: none"> COF area needs to be handled with care. <ul style="list-style-type: none"> GOOD → Wire path design to system side. OK → Wire path is located between COFs. BAD → Wire path overlapped with COF area. |

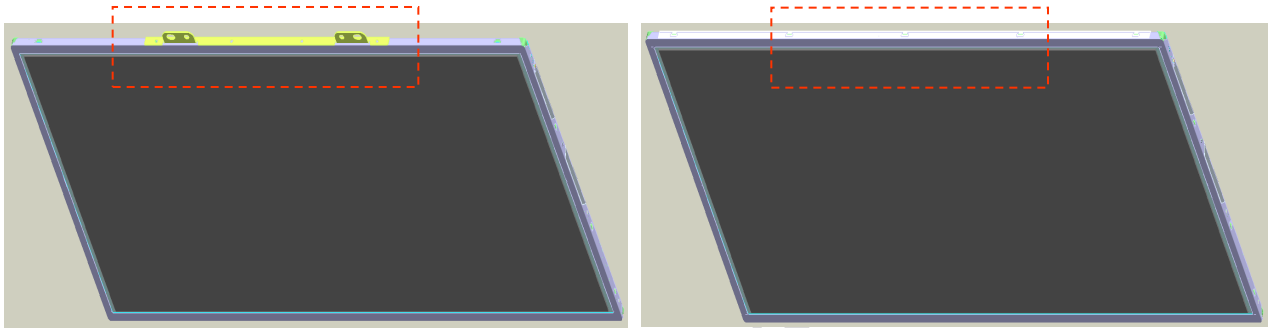
Product Specification

APPENDIX A. LGD Proposal for system cover design

| | |
|---|--|
| 5 | Using a bracket on the top of LCM is not recommended. |
|---|--|

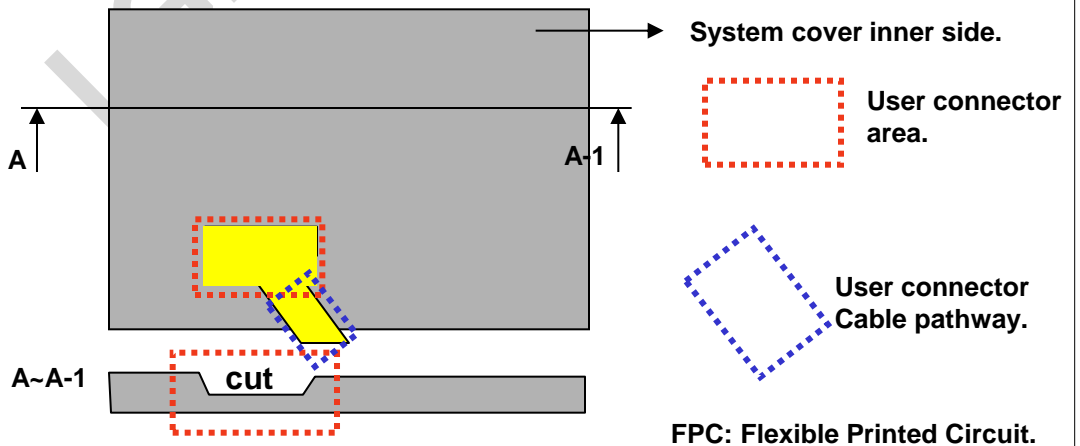


bracket



| | |
|--------|--|
| Define | 1. Condition without bracket is good for mechanical noise, and can minimize the light leakage from deformation of bracket. |
| | 2. The results shows that there is no difference between the condition with or without bracket. |

| | |
|---|---|
| 6 | Securing additional gap on CNT area. |
|---|---|



| | |
|--------|---|
| Define | <p>1. CNT area is specially sensitive against external stress, and additional gap by cutting on system cover will be helpful on removing the Ripple.</p> <p>2. Using a thinner CNT will be better. (e.g.: FPC type)</p> |
|--------|---|

APPENDIX A. LGD Proposal for system cover design

| | |
|---|---|
| 7 | Check mouse pad (touch pad) depth and shape of edge |
|---|---|

Mouse pad

[OK] $a \leq 0.3\text{mm}$
 [CO] $0.5\text{mm} \geq a \geq 0.3\text{mm}$
 [NG] $a \geq 0.5\text{mm}$

OK

NG

| | |
|--------|--|
| Define | 1. Mouse pad step is deep, it is caused panel crack by external load. 2. The edge shape must be smooth. |
|--------|--|

| | |
|---|---------------------------------|
| 8 | Check the step of keyboard area |
|---|---------------------------------|

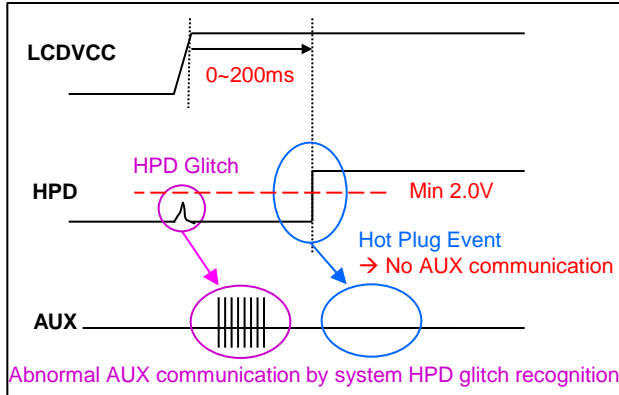
OK

NG

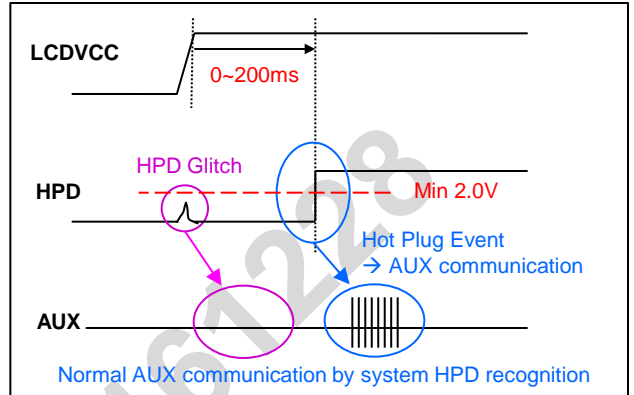
| | |
|--------|--|
| Define | The step of keyboard at the side edge of main body, it is caused panel crack |
|--------|--|

APPENDIX B. LGD Proposal for eDP Interface Design Guide

1 HPD Signal recognition



[Abnormal Communication By HPD Glitch]

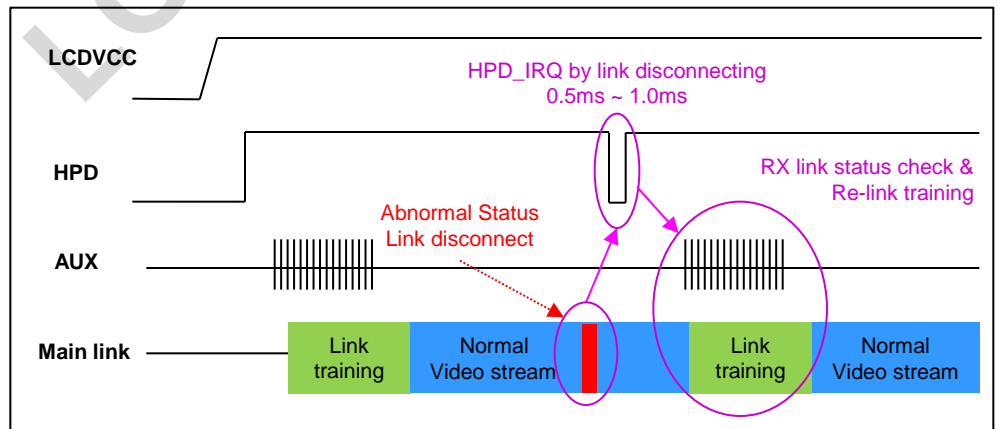


[Normal Communication By HPD Signal]

- Define
1. Hot Plug Detection (HPD) Threshold level of Source Device is minimum 2.0V
 2. HPD Unplug : HPD pulse stays low longer than 2ms.
DP Tx shall wait for HPD signal to go high again.
 3. "HPD High" is confirmed only after HPD has been asserted continuously for 100msec.

2 IRQ (Interrupt Request) HPD Pulse Definition

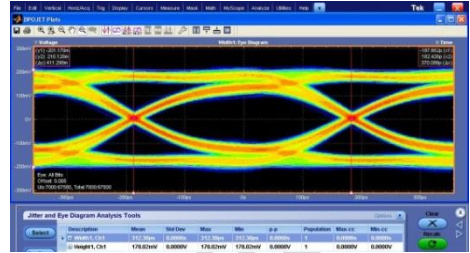
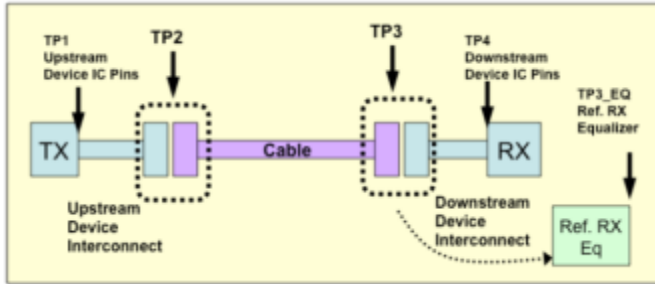
Ex) HPD Pulse



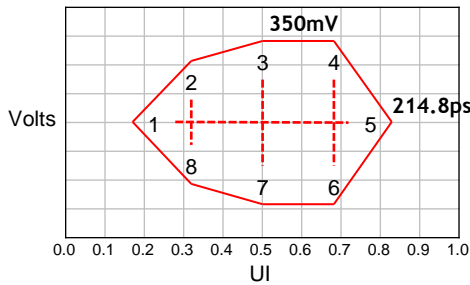
- Define
- Upon detection this "HPD IRQ Event"(0.5ms ~ 1ms) ,the source device must read the link / sink status field of the DPCD and take corrective action.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

3 Main Link EYE Diagram

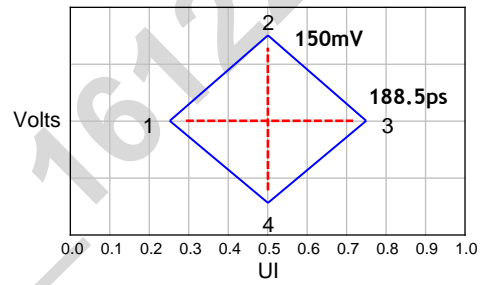


[EYE Diagram]



| Point | UI | Voltage (Volts) |
|-------|-------|-----------------|
| 1 | 0.210 | 0.000 |
| 2 | 0.355 | 0.140 |
| 3 | 0.500 | 0.175 |
| 4 | 0.645 | 0.175 |
| 5 | 0.790 | 0.000 |
| 6 | 0.645 | -0.175 |
| 7 | 0.500 | -0.175 |
| 8 | 0.355 | -0.140 |

[EYE Vertices for TP2 at HBR]

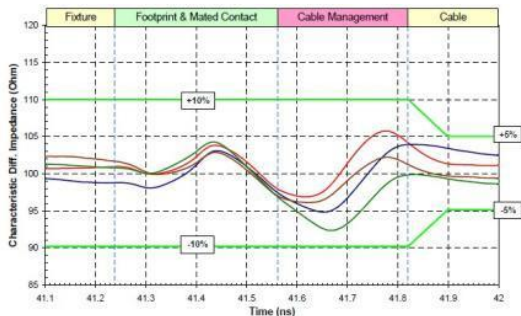


| Point | UI | Voltage (Volts) |
|-------|-------|-----------------|
| 1 | 0.246 | 0.000 |
| 2 | 0.500 | 0.075 |
| 3 | 0.755 | 0.000 |
| 4 | 0.500 | -0.075 |

[EYE Vertices for TP3 at HBR]

Define Main Link EYE Diagram should meet TP2 and TP3 point

4 Cable Impedance management

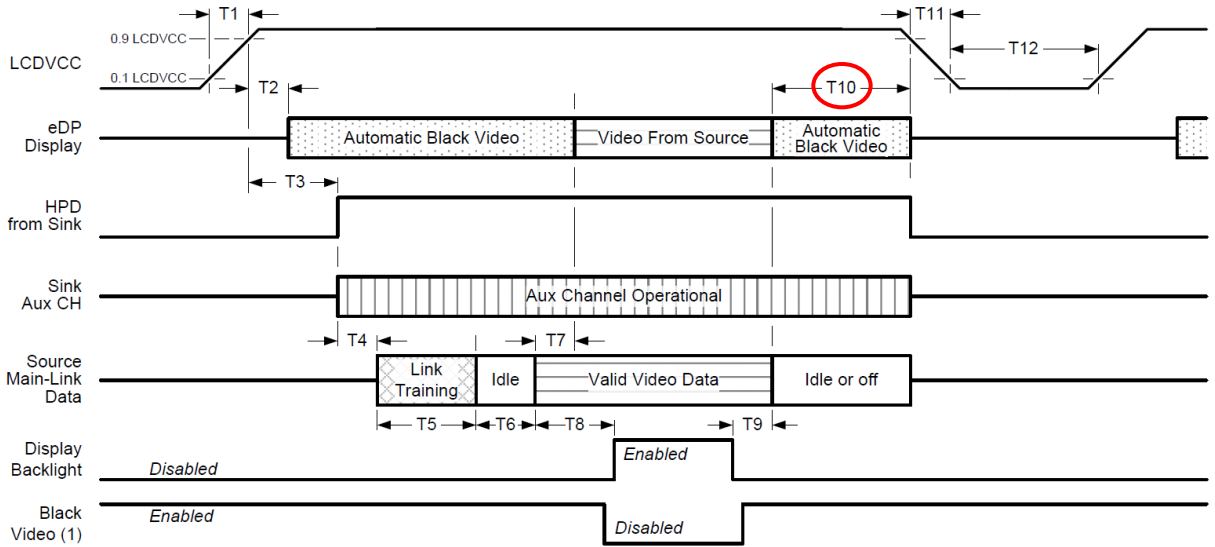


| Segment | Differential Impedance | Maximum Tolerance |
|-----------------|------------------------|-------------------|
| Fixture | 100 Ω | +/- 10% |
| Connector | 100 Ω | |
| Wire management | 100 Ω | |
| Cable | 100 Ω | +/- 5% |

Define Cable Impedance 100 Ω +/- 5% (95Ω ~ 105Ω)

APPENDIX B. LGD Proposal for eDP Interface Design Guide

5 Main Link Off vs. LCD Power Off at Non-PSR



| Timing Parameter | Description | Required By | Min | Max |
|------------------|--|-------------|-----|-------|
| T10 | Delay from end of valid video from Source to Power Off | Source | 0ms | 500ms |

* LGD recommend that Source must power off the LCDVCC if Main Link off like below.



[Case1. Resolution Change]



[Case2. Close the Lid]

Define

If Main Link off signal from Source, then LCDVCC must be Power Off within T10 period at Non-PSR mode

APPENDIX B. LGD Proposal for eDP Interface Design Guide

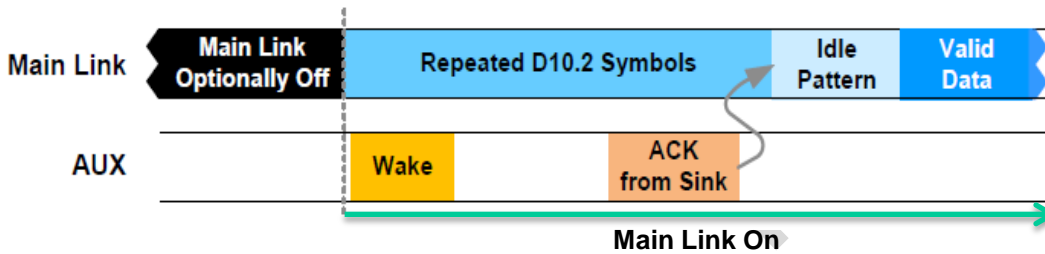
| | |
|---|---|
| 6 | Main Link M & N value of MSA data |
| <p>The diagram shows the timing of the eDP interface signals. LCDVCC rises first. HPD then goes high. On the AUX line, a Training Pattern 1 is transmitted. On the Main link, TP1 and TP2 are transmitted, followed by five video frames (1st Frame to 5th Frame). A red dashed box highlights the Link Training period between TP1 and TP2. A grey box labeled 'Main Stream Attribute (MSA) Data' is shown below the frames, with arrows pointing to the start of each frame. Text below the diagram lists video timing and pixel frequency information.</p> <p>-Video Timing : Htotal, Vtotal, Hwidth, Hstart, Vstart, Hsync width, Hsync polarity , etc.. -Pixel Freq. information : M & N Value</p> | |
| Define | It need to fix M& N value of MSA data output to prevent the initial abnormal M& N Value from incoming after power on. |

APPENDIX B. LGD Proposal for eDP Interface Design Guide

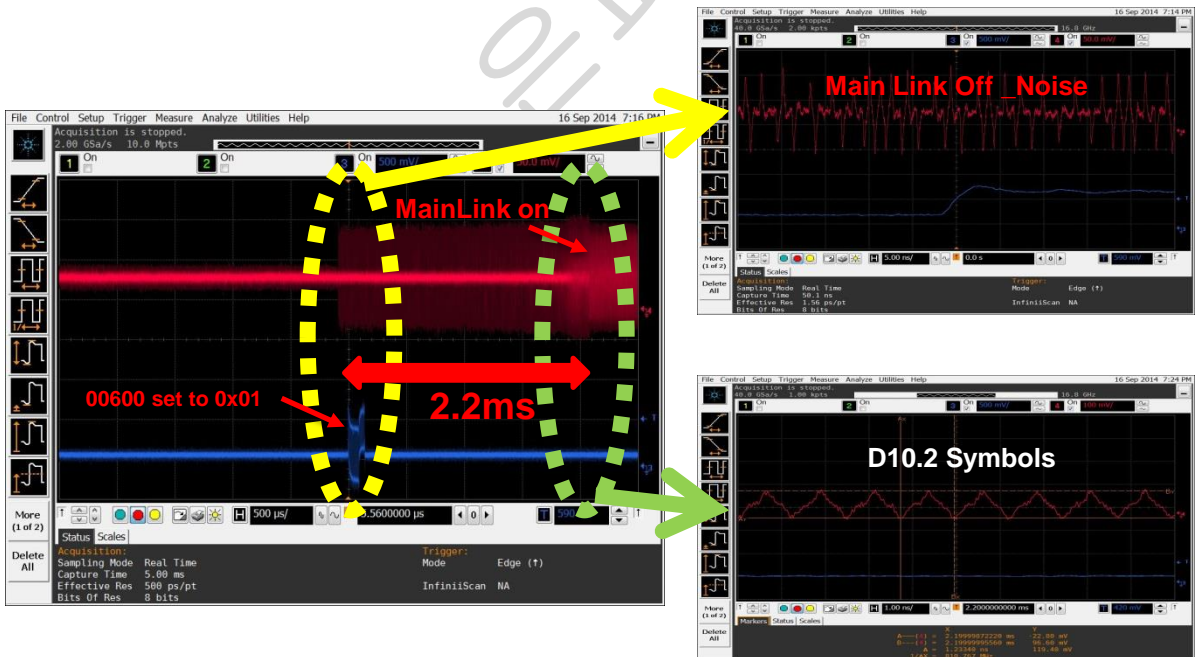
7 PSR Exit

If link training is not required, the Source must begin transmitting data on the Main Link prior to the wake AUX command which occurs through writing 01h to the SET_POWER & SET_DP_PWR_VOLTAGE register (DPCD Address 00600h; see DP v1.2a), as illustrated in the upper portion of Figure 6-9. This transmitted data must be a repetition of D10.2 symbols (which is the same as Link Training Pattern 1). Note the requirement above to transmit five repeats of the Idle Pattern after receiving ACK from the Sink.

PSR Exit Link Management with No Link Training



- The below waveform is the issued case.

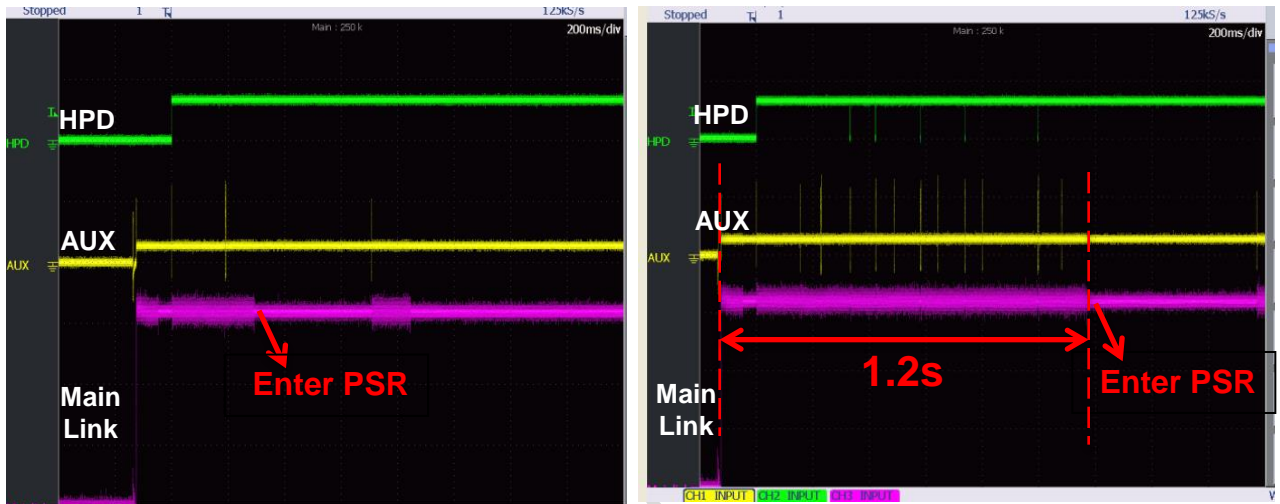


Define

If link training is not required, the source must begin transmitting data on the ML prior to the wake AUX wake-up command.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

8 1st time PSR Entry after Power on



< Issue waveform >

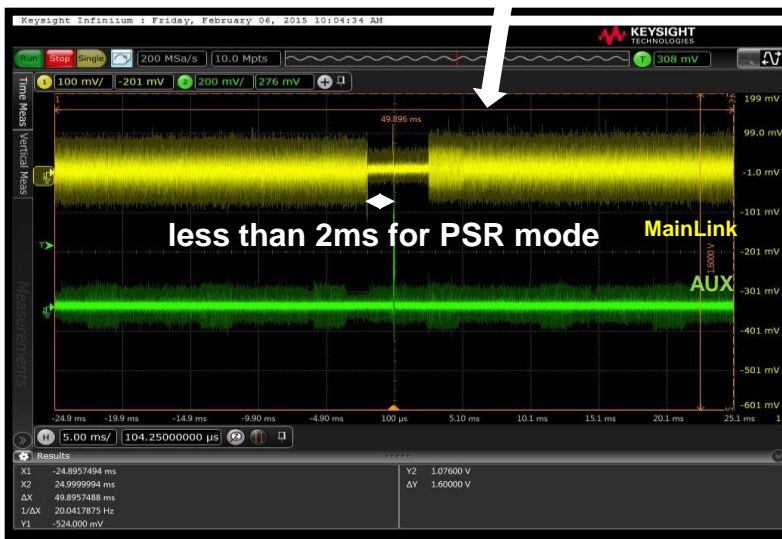
< solution waveform >

1. It is found that with solution , the TCON enter the PSR timing is 1.2s delay from VCC on which avoid TCON capture the wrong data from DP link(poor link quality) and enter the BIST mode + PSR mode(black screen).
2. According to test, link is stable 800ms after VCC on.

Define After power(Vcc) on, the DP link is not stable, so the source try to PSR entry at 800ms after Power(Vcc) on..

APPENDIX B. LGD Proposal for eDP Interface Design Guide

9 PSR Period Issue

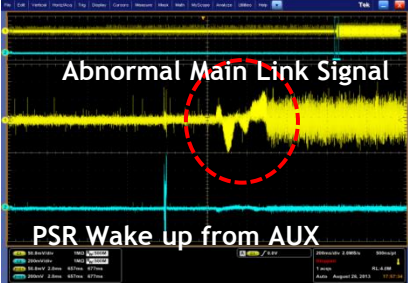
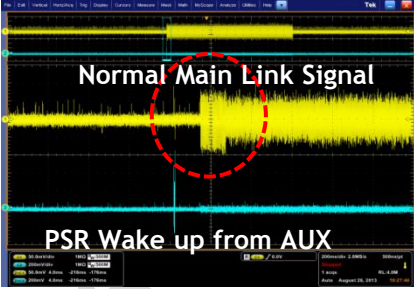


1. When issue is happened, system go to PSR mode for very short time.
2. If PSR active period is shorter than 1frame(16.67ms), T-Con can not go to the standby mode for PSR exit.

Define

When GPU go to the PSR mode, the source must hold the main link off over than 1frame.

APPENDIX B. LGD Proposal for eDP Interface Design Guide

| | |
|---|---|
| 10 | Main Link Noise at PSR Exit |
| <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;">  <p>Abnormal Main Link Signal</p> <p>PSR Wake up from AUX</p> <p>[Abnormal Main Link Noise]</p> </div> <div style="text-align: center;">  <p>Normal Main Link Signal</p> <p>PSR Wake up from AUX</p> <p>[Normal Main Link Signal]</p> </div> </div> | |
| Define | Main Link Noise at PSR Exit mode can be a cause abnormal display. |

Product Specification

APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 1/3

| | Byte (Dec) | Byte (Hex) | Field Name and Comments | Value (Hex) | Value (Bin) |
|--------------------------------------|------------|---|---|-------------|-------------|
| Header | 0 | 00 | Header | 00 | 00000000 |
| | 1 | 01 | Header | FF | 11111111 |
| | 2 | 02 | Header | FF | 11111111 |
| | 3 | 03 | Header | FF | 11111111 |
| | 4 | 04 | Header | FF | 11111111 |
| | 5 | 05 | Header | FF | 11111111 |
| | 6 | 06 | Header | FF | 11111111 |
| | 7 | 07 | Header | 00 | 00000000 |
| Vendor / Product EDID Version | 8 | 08 | ID Manufacture Name LGD | 30 | 00110000 |
| | 9 | 09 | ID Manufacture Name | E4 | 11100100 |
| | 10 | 0A | ID Product Code 0542h | 42 | 01000010 |
| | 11 | 0B | (Hex LSB first) | 05 | 00000101 |
| | 12 | 0C | ID Serial No. - Optional ("00h" If not used, Number Only and LSB First) | 00 | 00000000 |
| | 13 | 0D | ID Serial No. - Optional ("00h" If not used, Number Only and LSB First) | 00 | 00000000 |
| | 14 | 0E | ID Serial No. - Optional ("00h" If not used, Number Only and LSB First) | 00 | 00000000 |
| | 15 | 0F | ID Serial No. - Optional ("00h" If not used, Number Only and LSB First) | 00 | 00000000 |
| | 16 | 10 | Week of Manufacture - Optinal 00 weeks | 00 | 00000000 |
| | 17 | 11 | Year of Manufacture 2016 years | 1A | 00011010 |
| | 18 | EDID structure version # = 1 | 01 | 00000001 | |
| | 19 | EDID revision # = 4 | 04 | 00000100 | |
| Display Parameters | 20 | 14 | Video input Definition = Input is a Digital Video signal Interface , Colo Bit Depth : 6 Bits per Primary Color , Digital Video Interface Standard Supported: DisplayPort is supported | 95 | 10010101 |
| | 21 | 15 | Horizontal Screen Size (Rounded cm) = 28 cm | 1C | 00011100 |
| | 22 | 16 | Vertical Screen Size (Rounded cm) = 16 cm | 10 | 00010000 |
| | 23 | 17 | Display Transfer Characteristic (Gamma) = (gamma*100)-100 = Example:(2.2*100)-100=120 | 78 | 01111000 |
| | 24 | 18 | Feature Support [Display Power Management(DPM) : Standby Mode is not supported, Suspend Mode is not supported, Active Off = Very Low Power is not supported ,Supported Color Encoding Formats : RGB 4:4:4 ,Other Feature Support Flags : No_sRGB, Preferred Timing Mode, No_Display is continuous frequency (Multi-mode_Base EDID and Extension Block).] | 02 | 00000010 |
| Panel Color Coordinates | 25 | 19 | Red/Green Low Bits (RxRy/GxGy) | DF | 11011111 |
| | 26 | 1A | Blue/White Low Bits (BxBY/WxWy) | 25 | 00100101 |
| | 27 | 1B | Red X Rx = 0.589 | 96 | 10010110 |
| | 28 | 1C | Red Y Ry = 0.356 | 5B | 01011011 |
| | 29 | 1D | Green X Gx = 0.335 | 55 | 01010101 |
| | 30 | 1E | Green Y Gy = 0.565 | 90 | 10010000 |
| | 31 | 1F | Blue X Bx = 0.156 | 28 | 00101000 |
| | 32 | 20 | Blue Y By = 0.104 | 1A | 00011010 |
| | 33 | White X Wx = 0.313 | 50 | 01010000 | |
| | 34 | White Y Wy = 0.329 | 54 | 01010100 | |
| Established Timings | 35 | 23 | Established timing 1 (Optional_00h if not used) | 00 | 00000000 |
| | 36 | 24 | Established timing 2 (Optional_00h if not used) | 00 | 00000000 |
| | 37 | 25 | Manufacturer's timings (Optional_00h if not used) | 00 | 00000000 |
| Standard Timing ID | 38 | 26 | Standard timing ID1 (Optional_01h if not used) | 01 | 00000001 |
| | 39 | 27 | Standard timing ID1 (Optional_01h if not used) | 01 | 00000001 |
| | 40 | 28 | Standard timing ID2 (Optional_01h if not used) | 01 | 00000001 |
| | 41 | 29 | Standard timing ID2 (Optional_01h if not used) | 01 | 00000001 |
| | 42 | 2A | Standard timing ID3 (Optional_01h if not used) | 01 | 00000001 |
| | 43 | 2B | Standard timing ID3 (Optional_01h if not used) | 01 | 00000001 |
| | 44 | 2C | Standard timing ID4 (Optional_01h if not used) | 01 | 00000001 |
| | 45 | 2D | Standard timing ID4 (Optional_01h if not used) | 01 | 00000001 |
| | 46 | 2E | Standard timing ID5 (Optional_01h if not used) | 01 | 00000001 |
| | 47 | 2F | Standard timing ID5 (Optional_01h if not used) | 01 | 00000001 |
| | 48 | 30 | Standard timing ID6 (Optional_01h if not used) | 01 | 00000001 |
| | 49 | 31 | Standard timing ID6 (Optional_01h if not used) | 01 | 00000001 |
| | 50 | 32 | Standard timing ID7 (Optional_01h if not used) | 01 | 00000001 |
| | 51 | 33 | Standard timing ID7 (Optional_01h if not used) | 01 | 00000001 |
| | 52 | 34 | Standard timing ID8 (Optional_01h if not used) | 01 | 00000001 |
| 53 | 35 | Standard timing ID8 (Optional_01h if not used) | 01 | 00000001 | |

Product Specification

APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 2/3

| | Byte (Dec) | Byte (Hex) | Field Name and Comments | Value (Hex) | Value (Bin) |
|----------------------|------------|---|---|-------------|-------------|
| Timing Descriptor #1 | 54 | 36 | Pixel Clock/10,000 (LSB) 138.7 MHz @ 60 Hz | 2E | 00101110 |
| | 55 | 37 | Pixel Clock/10,000 (MSB) | 36 | 00110110 |
| | 56 | 38 | Horizontal Active (HA) (lower 8 bits) 1920 pixels | 80 | 10000000 |
| | 57 | 39 | Horizontal Blanking (HB) (lower 8 bits) 160 pixels | A0 | 10100000 |
| | 58 | 3A | Horizontal Active (HA) / Horizontal Blanking (HB) (upper 4:4bits) | 70 | 01110000 |
| | 59 | 3B | Vertical Active (VA) 1080 lines | 38 | 00111000 |
| | 60 | 3C | Vertical Blanking (VB) (DE Blanking typ.for DE only panels) 31 lines | 1F | 00011111 |
| | 61 | 3D | Vertical Active (VA) / Vertical Blanking (VB) (upper 4:4bits) | 40 | 01000000 |
| | 62 | 3E | Horizontal Front Porch in pixels (HF) (lower 8 bits) 48 pixels | 30 | 00110000 |
| | 63 | 3F | Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits) 32 pixels | 20 | 00100000 |
| | 64 | 40 | Vertical Front Porch in lines (VF) : Vertical Sync Pulse Width in lines (VS) (lower 4 bits) 3 lines : 5 lines | 35 | 00110101 |
| | 65 | 41 | Horizontal Front Porch/ Sync Pulse Width/ Vertical Front Porch/ Sync Pulse Width (upper 2bits) | 00 | 00000000 |
| | 66 | 42 | Horizontal Vedio Image Size (mm) (lower 8 bits) 276 mm | 14 | 00010100 |
| | 67 | 43 | Vertical Vedio Image Size (mm) (lower 8 bits) 156 mm | 9C | 10011100 |
| 68 | 44 | Horizontal Image Size / Vertical Image Size (upper 4 bits) | 10 | 00010000 | |
| 69 | 45 | Horizontal Border = 0 (Zero for Notebook LCD) | 00 | 00000000 | |
| 70 | 46 | Vertical Border = 0 (Zero for Notebook LCD) | 00 | 00000000 | |
| 71 | 47 | Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_POS (outside of V-sync)] | 1A | 00011010 | |
| Timing Descriptor #2 | 72 | 48 | Pixel Clock/10,000 (LSB) 111 MHz @ 48 Hz | 5C | 01011100 |
| | 73 | 49 | Pixel Clock/10,000 (MSB) | 2B | 00101011 |
| | 74 | 4A | Horizontal Active (HA) (lower 8 bits) 1920 pixels | 80 | 10000000 |
| | 75 | 4B | Horizontal Blanking (HB) (lower 8 bits) 160 pixels | A0 | 10100000 |
| | 76 | 4C | Horizontal Active (HA) / Horizontal Blanking (HB) (upper 4:4bits) | 70 | 01110000 |
| | 77 | 4D | Vertical Active (VA) 1080 lines | 38 | 00111000 |
| | 78 | 4E | Vertical Blanking (VB) (DE Blanking typ.for DE only panels) 31 lines | 1F | 00011111 |
| | 79 | 4F | Vertical Active (VA) / Vertical Blanking (VB) (upper 4:4bits) | 40 | 01000000 |
| | 80 | 50 | Horizontal Front Porch in pixels (HF) (lower 8 bits) 48 pixels | 30 | 00110000 |
| | 81 | 51 | Horizontal Sync Pulse Width in pixels (HS) (lower 8 bits) 32 pixels | 20 | 00100000 |
| | 82 | 52 | Vertical Front Porch in lines (VF) : Vertical Sync Pulse Width in lines (VS) (lower 4 bits) 3 lines : 5 lines | 35 | 00110101 |
| | 83 | 53 | Horizontal Front Porch/ Sync Pulse Width/ Vertical Front Porch/ Sync Pulse Width (upper 2bits) | 00 | 00000000 |
| | 84 | 54 | Horizontal Vedio Image Size (mm) (lower 8 bits) 276 mm | 14 | 00010100 |
| | 85 | 55 | Vertical Vedio Image Size (mm) (lower 8 bits) 156 mm | 9C | 10011100 |
| 86 | 56 | Horizontal Image Size / Vertical Image Size (upper 4 bits) | 10 | 00010000 | |
| 87 | 57 | Horizontal Border = 0 (Zero for Notebook LCD) | 00 | 00000000 | |
| 88 | 58 | Vertical Border = 0 (Zero for Notebook LCD) | 00 | 00000000 | |
| 89 | 59 | Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_POS (outside of V-sync)] | 1A | 00011010 | |
| Timing Descriptor #3 | 90 | 5A | Flag | 00 | 00000000 |
| | 91 | 5B | Flag | 00 | 00000000 |
| | 92 | 5C | Flag | 00 | 00000000 |
| | 93 | 5D | Data Type Tag : Alphanumeric Data String (ASCII String) | FE | 11111110 |
| | 94 | 5E | Flag | 00 | 00000000 |
| | 95 | 5F | Dell P/N 1st Character = D | 44 | 01000100 |
| | 96 | 60 | Dell P/N 2nd Character = N | 4E | 01001110 |
| | 97 | 61 | Dell P/N 3rd Character = D | 44 | 01000100 |
| | 98 | 62 | Dell P/N 4th Character = 8 | 38 | 00111000 |
| | 99 | 63 | Dell P/N 5th Character = T | 54 | 01010100 |
| | 100 | 64 | EDID Revision Build Name = MP(X-Build) , Revision # = A00 | 80 | 10000000 |
| | 101 | 65 | Manufacturer P/N = 1 | 31 | 00110001 |
| | 102 | 66 | Manufacturer P/N = 2 | 32 | 00110010 |
| | 103 | 67 | Manufacturer P/N = 5 | 35 | 00110101 |
| 104 | 68 | Manufacturer P/N = W | 57 | 01010111 | |
| 105 | 69 | Manufacturer P/N = F | 46 | 01000110 | |
| 106 | 6A | Manufacturer P/N = 4 | 34 | 00110100 | |
| 107 | 6B | Manufacturer P/N (If < 13 char, then terminate with ASCII code 0Ah,set remaining char = 20h) | 0A | 00001010 | |

Product Specification

APPENDIX C. Enhanced Extended Display Identification Data (EEDID™) 3/3

| | Byte (Dec) | Byte (Hex) | Field Name and Comments | Value (Hex) | Value (Bin) |
|-----------------------------|------------|---|--|-------------|-------------|
| Timing Descriptor #4 | 108 | 6C | Flag | 00 | 00000000 |
| | 109 | 6D | Flag | 00 | 00000000 |
| | 110 | 6E | Flag | 00 | 00000000 |
| | 111 | 6F | Data Type Tag : Descriptor Defined by manufacturer | 00 | 00000000 |
| | 112 | 70 | Flag | 00 | 00000000 |
| | 113 | 71 | Color Management [No +2FRC Support, True Color Depth : 6 bit] | 00 | 00000000 |
| | 114 | 72 | Panel Type [WLED], Configuration [Single light bar], Number Lamp or LED Light Bar [one] | 41 | 01000001 |
| | 115 | 73 | Frame Rate Details [Minimum Frame Rate : 40Hz, Maximum Frame Rate : 65Hz , Tcon provides native Intel DRRS / sDRRS support] | 31 | 00110001 |
| | 116 | 74 | Controller Interface and Maximum Luminance [PWM type, 300 nit] | 9E | 10011110 |
| | 117 | 75 | Front Surface / Polarizer [Anti-Glare, No Transflective], Pixel Structure [RGB v-stripe] | 00 | 00000000 |
| | 118 | 76 | Multi-Media Features [Color Management : NTSC, Dynamic Backlight Control : Type 1] | 10 | 00010000 |
| | 119 | 77 | Multi-Media Features [Motion Blur : No support , Active Gamma Control : No support] | 00 | 00000000 |
| | 120 | 78 | Special Features [Wireless Enhancement Hardware : No support , In-Cell Scanner : No support] | 00 | 00000000 |
| | 121 | 79 | Special Features [Number of LVDS channels or eDP lanes : two , Overdrive : No ,Interface : eDP , In-Cell Touch Support : No] | 0A | 00001010 |
| | 122 | 7A | Special Features [BIST Support : yes , Electronic Privacy : No electronic privacy hardware support , 3-D Support : No] | 01 | 00000001 |
| 123 | 7B | (If<13 char--> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h) | 0A | 00001010 | |
| 124 | 7C | (If<13 char--> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h) | 20 | 00100000 | |
| 125 | 7D | (If<13 char--> 0Ah, then terminate with ASC II code 0Ah,set remaining char = 20h) | 20 | 00100000 | |
| Checksum | 126 | 7E | Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0) | 00 | 00000000 |
| | 127 | 7F | Check Sum(The 1-byte sum of all 128 bytes in this panel ID block shall = 0) | C2 | 11000010 |

Our company network supports you worldwide with offices in Germany, Austria, Switzerland, the UK and the USA. For more information please contact:

Headquarters

Germany



FORTEC Elektronik AG

Lechwiesenstr. 9
86899 Landsberg am Lech

Phone: +49 8191 91172-0
E-Mail: sales@forteca.de
Internet: www.forteca.de

Fortec Group Members

Austria



FORTEC Elektronik AG

Office Vienna

Nuschinggasse 12
1230 Wien

Phone: +43 1 8673492-0
E-Mail: office@fortec.at
Internet: www.fortec.at

Germany



Distec GmbH

Augsburger Str. 2b
82110 Germering

Phone: +49 89 894363-0
E-Mail: info@distec.de
Internet: www.distec.de

Switzerland



ALTRAC AG

Bahnhofstraße 3
5436 Würenlos

Phone: +41 44 7446111
E-Mail: info@altrac.ch
Internet: www.altrac.ch

United Kingdom



Display Technology Ltd.

Osprey House, 1 Osprey Court
Hichingbrooke Business Park
Huntingdon, Cambridgeshire, PE29 6FN

Phone: +44 1480 411600
E-Mail: info@displaytechnology.co.uk
Internet: www.displaytechnology.co.uk

USA



Apollo Display Technologies, Corp.

87 Raynor Avenue,
Unit 1 Ronkonkoma,
NY 11779

Phone: +1 631 5804360
E-Mail: info@apolloDisplays.com
Internet: www.apolloDisplays.com