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Datasheet

KOE

TX27D200VM0AAA

KO-01-007

TENTATIVE

KOE

JDI Group

Kaohsiung Opto-Electronics Inc.

FOR MESSRS : _____ DATE : Aug. 5th ,2020

TECHNICAL DATA

TX27D200VM0AAA

Contents

ACCEPTED BY: _____ PROPOSED BY: John Chou

2. RECORD OF REVISION

DATE	SHEET No.	SUMMARY

3. GENERAL DATA

3.1 DISPLAY FEATURES

This module is a 10.6” WXGA of 16:9 format amorphous silicon TFT. The pixel format is vertical stripe and sub pixels are arranged as R(red), G(green), B(blue) sequentially. This display is RoHS compliant, and COG (chip on glass) technology and LED backlight are applied on this display.

Part Name	TX27D200VM0AAA
Module Dimensions	250.0 (W) mm × 157.0 (H) mm × 8.9 (D) mm (Typ.)
LCD Active Area	231.36 (W)mm x 138.816(H)mm
Pixel Pitch	0.18075 (W) mm × 0.18075 (H) mm
Resolution	1280× 3 (RGB) (W) × 768 (H) dots
Color Pixel Arrangement	RGB Vertical Stripe
LCD Type	Transmissive Type, Normally Black
Display Type	Active Matrix
Number of Colors	262K (6-bit RGB) / 16.2M(6-bit RGB + FRC) / 16.7M (8-bit RGB) Colors
Backlight	Light Emitting Diode (LED)
Weight	TBDg (typ)
Interface	LVDS；20pins
Power Supply Voltage	3.3V for LCD；21V for Backlight
Viewing Direction	Super Wide Version

4. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	V_{DD}	-0.3	4.0	V	-
Input Voltage of Logic	V_I	-0.3	4.0	V	Note 1
Operating Temperature	Top	-40	85	°C	Note 2
Storage Temperature	Tst	-40	90	°C	Note 2
Backlight Input Voltage	V_{LED}	-	23.8	V	-

Note 1: The rating is defined for the signal voltage of the interface such as CLK and pixel data pairs.

Note 2: The maximum rating is defined as above based on the panel surface temperature, which might be different from ambient temperature after assembling the panel into the application. Moreover, some temperature-related phenomenon as below needed to be noticed:

- Background color, contrast and response time would be different in temperatures other than 25 °C.
- Operating under high temperature will shorten LED lifetime.

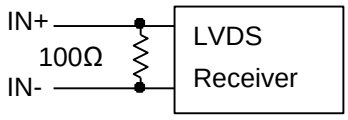
5. ELECTRICAL CHARACTERISTICS

5.1 LCD CHARACTERISTICS

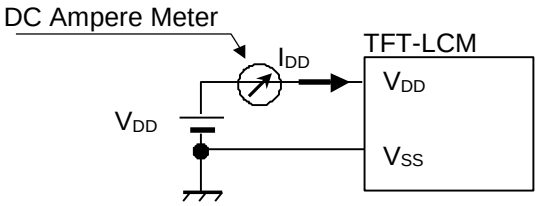
$T_a = 25\ ^{\circ}C,\ V_{SS} = 0V$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-	3.0	3.3	3.6	V	-
Differential Input Voltage for LVDS Receiver Threshold	V_I	V_{IH}	-	-	+100	mV	Note 1
		V_{IL}	-100	-	-		
Power Supply Current	I_{DD}	V_{DD}-V_{SS} =3.3V	-	TBD	TBD	mA	Note 2,3
Frame Frequency	f_{Frame}	-	-	60	-	Hz	Note 4
CLK Frequency	f_{CLK}	-	-	68.3	-	MHz	

Note 1: VCM 1.2V is common mode voltage of LVDS transmitter and receiver. The input terminal of LVDS transmitter is terminated with 100Ω.



Note 2: An all white check pattern is used when measuring I_{DD}. f_{Frame} is set to 60Hz.



Note 3: (TBD) fuse is applied in the module for I_{DD}. For display activation and protection purpose, power supply is recommended larger than (TBD) to start the display and break fuse once any short circuit occurred.

Note 4: For LVDS transmitter input.

5.2 BACKLIGHT CHARACTERISTICS

$T_a = 25\ ^\circ C$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
LED Input Voltage	VLED	Backlight Unit	-	21	-	V	Note 1
LED Forward Current	ILED	Backlight Unit	-	87	-	mA	-
LED Lifetime	-	87 mA	-	100K	-	hrs	Note 2

Note 1: Fig. 5.1 shows the LED backlight circuit. The circuit has 28 LEDs in total.

Note 2: The estimated lifetime is specified as the time to reduce 50% brightness by applying 87 mA at 25°C.

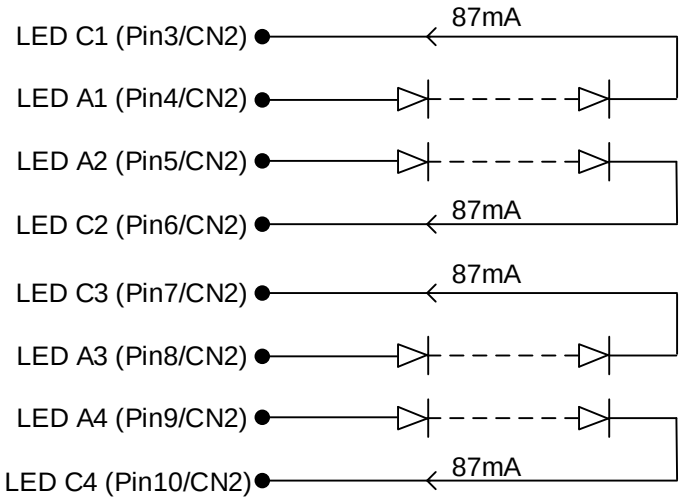


Fig 5.1

6. OPTICAL CHARACTERISTICS

The optical characteristics are measured based on the conditions as below:

- Supplying the signals and voltages defined in the section of electrical characteristics.
- The ambient temperature is 25°C.
- In the dark room less than 100 lx, the equipment has been set for the measurements as shown in Fig 6.1.

$T_a = 25\ ^{\circ}C$, $f_{Frame} = 60$ Hz, $V_{DD} = 3.3$V

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Brightness of White		-	I_{LED}= 348mA $\phi = 0^{\circ}, \theta = 0^{\circ}$	800	1000	-	cd/m^2	Note 1
Brightness Uniformity		-		70	-	-	%	Note 2
Contrast Ratio		CR		650	1000	-	-	Note 3
Response Time		Tr + Tf	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	24	-	ms	Note 4
NTSC Ratio		-	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	50	-	%	-
Viewing Angle		θ x	$\phi = 0^{\circ}$, CR ≥ 10	-	85	-	Degree	Note 5
		θ x′	$\phi = 180^{\circ}$, CR ≥ 10	-	85	-		
		θ y	$\phi = 90^{\circ}$, CR ≥ 10	-	85	-		
		θ y′	$\phi = 270^{\circ}$, CR ≥ 10	-	85	-		
Color Chromaticity	Red	X	$\phi = 0^{\circ}, \theta = 0^{\circ}$	-	0.581	-	-	Note 6
		Y		-	0.319	-		
	Green	X		-	0.334	-		
		Y		-	0.582	-		
	Blue	X		-	0.150	-		
		Y		-	0.131	-		
	White	X		-	0.313	-		
		Y		-	0.329	-		

Note 1: The brightness is measured from the center point of the panel, P5 in Fig. 6.2, for the typical value.

Note 2: The brightness uniformity is calculated by the equation as below:

$$\text{Brightness uniformity} = \frac{\text{Min. Brightness}}{\text{Max. Brightness}} \text{ X100\%}$$

which is based on the brightness values of the 9 points measured by BM-5 as shown in Fig. 6.2.

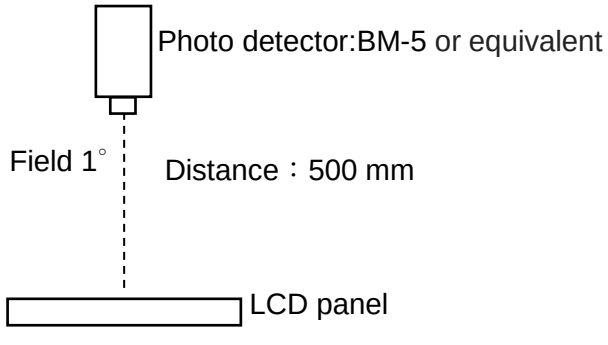


Fig. 6.1

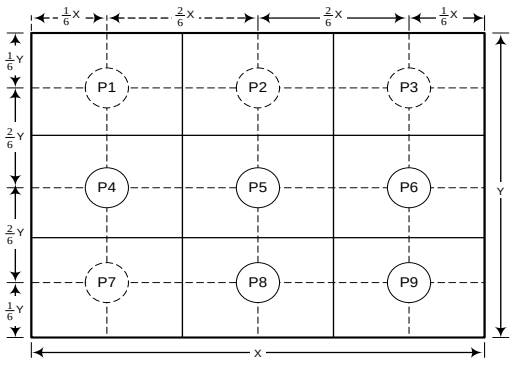


Fig. 6.2

Note 3: The Contrast ratio is measured from the center point of the panel, P5, and defined as the following equation:

$$CR = \frac{\text{Brightness of White}}{\text{Brightness of Black}}$$

Note 4: The definition of response time is shown in Fig. 6.3. The rising time is the period from 10% brightness to 90% brightness when the data is from black to white. Oppositely, Falling time is the period from 90% brightness rising to 10% brightness.

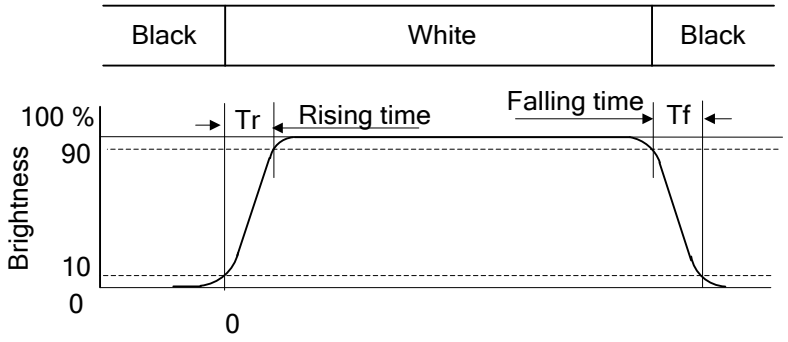


Fig. 6.3

Note 5: The definition of viewing angle is shown in Fig. 6.4. Angle ϕ is used to represent viewing directions, for instance, $\phi = 270^\circ$ means 6 o'clock, and $\phi = 0^\circ$ means 3 o'clock. Moreover, angle θ is used to represent viewing angles from axis Z toward plane XY.

The display is super wide viewing angle version, so that the best optical performance can be obtained from every viewing direction.

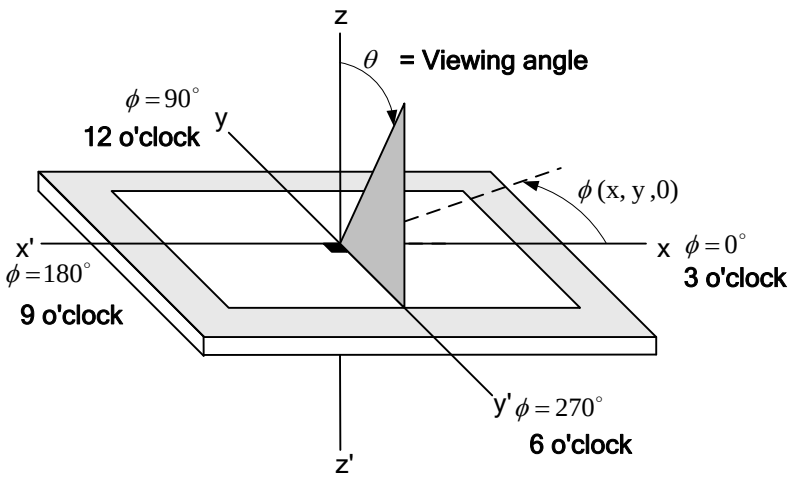
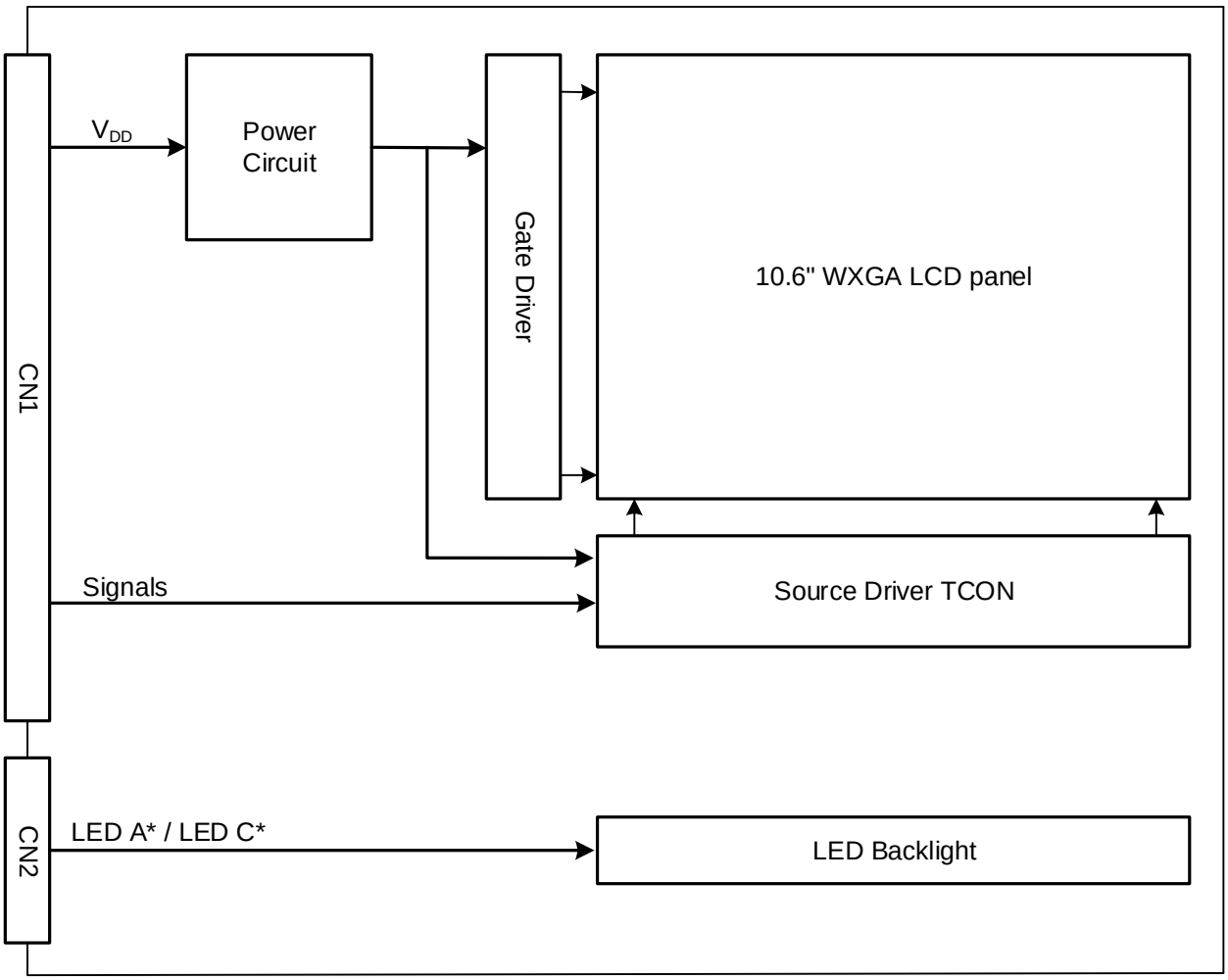


Fig. 6.4

Note 6: The color chromaticity is measured from the center point of the panel, P5, as shown in Fig. 6.2.

7. BLOCK DIAGRAM



Note :1 Signals are UD/LR, CLK and pixel data pairs.

8. LCD INTERFACE

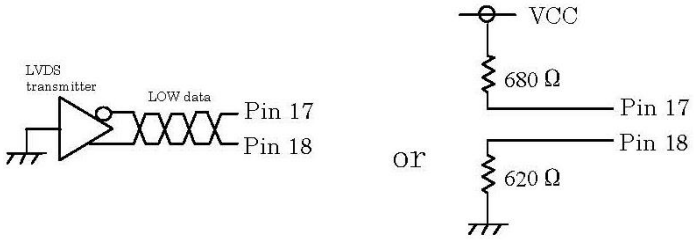
8.1 INTERFACE PIN CONNECTIONS

The display interface connector (CN1) is FI-SE20P-HFE made by JAE and pin assignment is as below:

Pin No.	Signal	Function (6 bit mode)		Function (8 bit mode)
		6 bit input	8 bit input	8 bit input
1	V_{DD}	+3.3V Power Supply for Logic		+3.3V Power Supply for Logic
2	V_{DD}	+3.3V Power Supply for Logic		+3.3V Power Supply for Logic
3	V_{SS}	GND		GND
4	V_{SS}	GND		GND
5	Link 0-	R0~R5, G0	R2~R7, G2	R0~R5, G0
6	Link 0+	R0~R5, G0	R2~R7, G2	R0~R5, G0
7	V_{SS}	GND		GND
8	Link 0-	G1~G5, B0~B1	G3~G7, B2~B3	G1~G5, B0~B1
9	Link 0+	G1~G5, B0~B1	G3~G7, B2~B3	G1~G5, B0~B1
10	V_{SS}	GND		GND
11	Link 2-	B2~B5, DE	B4~B7, DE	B2~B5, DE
12	Link 2+	B2~B5, DE	B4~B7, DE	B2~B5, DE
13	V_{SS}	GND		GND
14	CLK IN-	Pixel Clock -		Pixel Clock -
15	CLK IN+	Pixel Clock +		Pixel Clock +
16	V_{SS}	GND		GND
17	Link 3-	See:*2)	R0~R1, G0~G1, B0~B1	R6~R7, G6~G7, B6~B7
18	Link 3+	See:*2)	R0~R1, G0~G1, B0~B1	R6~R7, G6~G7, B6~B7
19	MODE	Low=ISP 6bit compatibility mode		High=ISP 6bit compatibility mode
20	UD/LR	Scan direction control (Low = Normal, High = Reverse)		

Note 1: Link n- and Link n+ (n=0, 1, 2, 3), CLK IN- and CLK IN+ should be wired by twist-pairs.

Note 2: Recommended wiring of Pin 17,18(6 bit input)

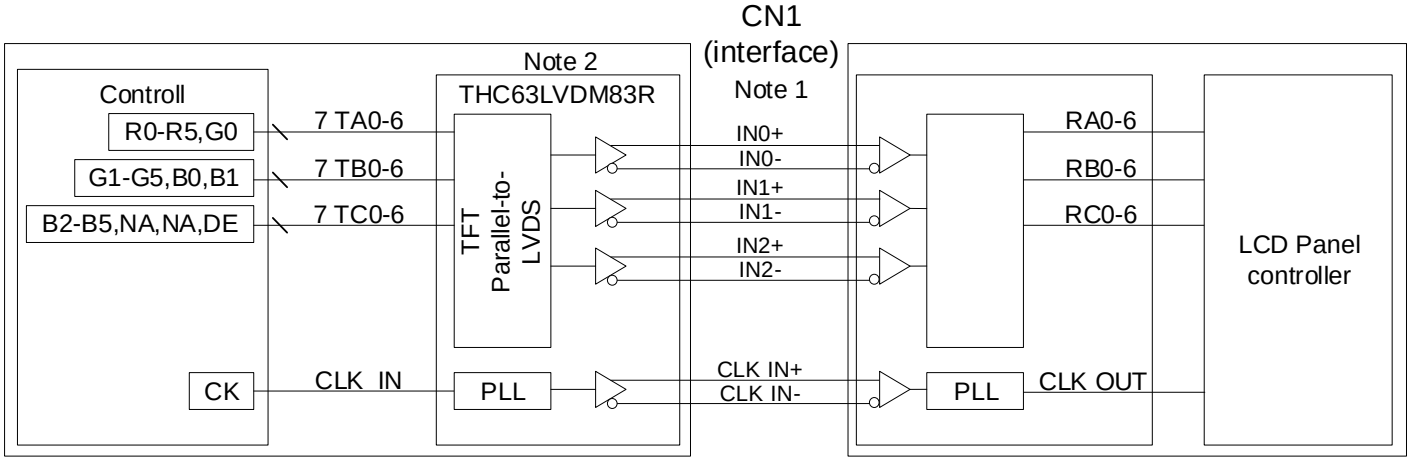


The display interface connector (CN2) is SM10B-SHLS-TF made by JST and pin assignment is as below:

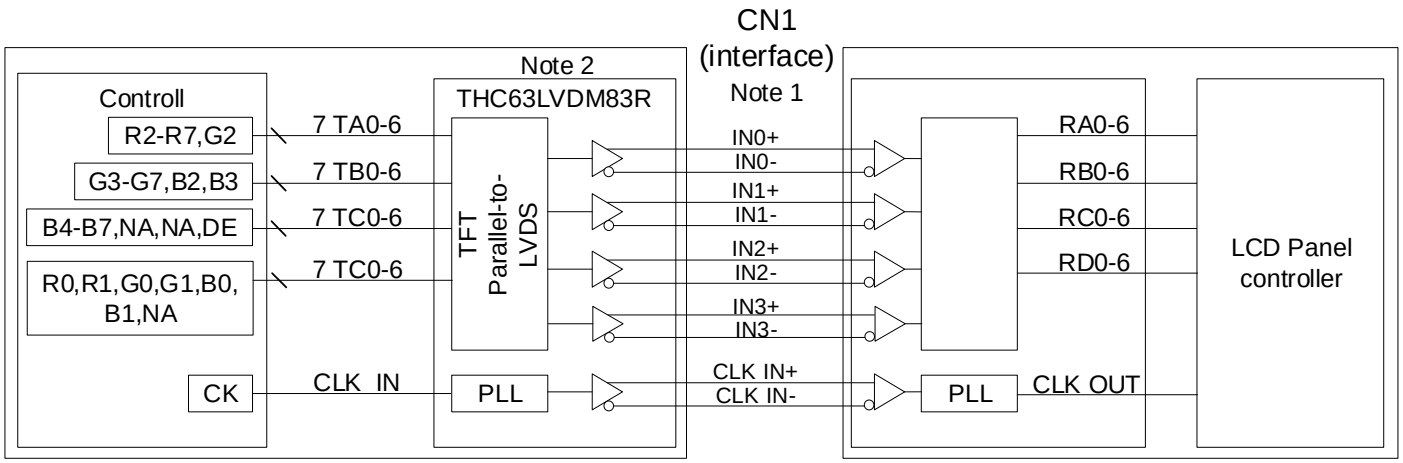
Pin No.	Symbol	Function
1	NC	This pin should be open.
2	NC	This pin should be open.
3	LED C1	LED catfode1
4	LED A1	LED anode1
5	LED A2	LED anode2
6	LED C2	LED catfode2
7	LED C3	LED catfode3
8	LED A3	LED anode3
9	LED A4	LED anode4
10	LED C4	LED catfode4

8.2 LVDS INTERFACE

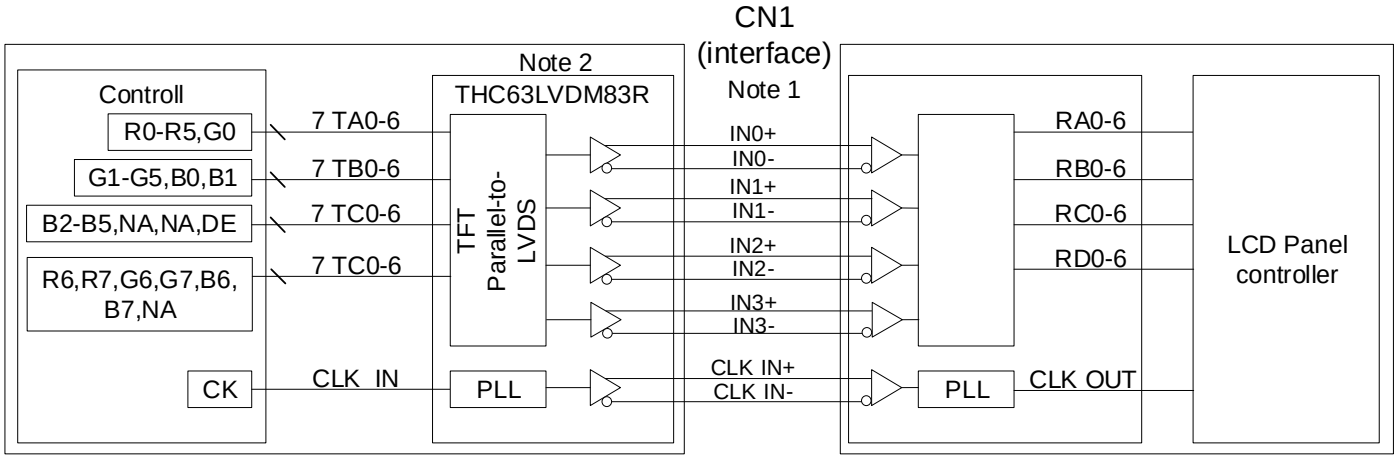
8.2.1 ISP 6 bit compatibility mode(6 bit input)



8.2.2 ISP 6 bit compatibility mode(8 bit input)



8.2.3 ISP 8 bit compatibility mode

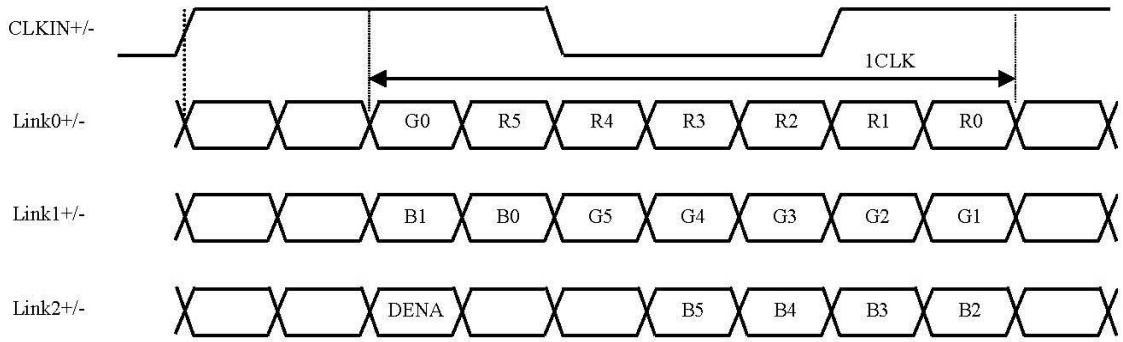


Note 1: LVDS cable impedance should be 100 ohms per signal line when each 2-lines (+, -) is used in differential mode.

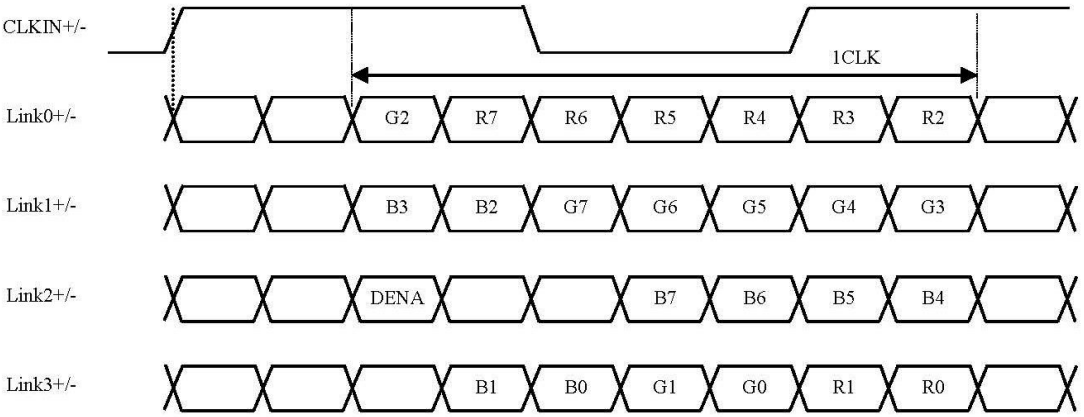
Note 2: The recommended transmitter, THC63LVDM83R, is made by Thine or equivalent, which is not contained in the module.

8.3 LVDS DATA FORMAT

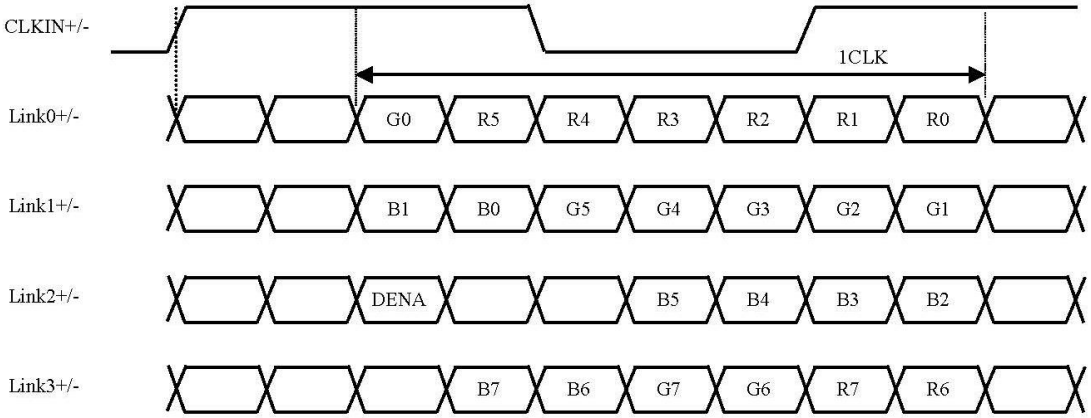
8.3.1 ISP 6 bit compatibility mode(6 bit input)



8.3.2 ISP 6 bit compatibility mode(8 bit input)



8.3.3 ISP 8 bit compatibility mode



8.4 TIMING CHART

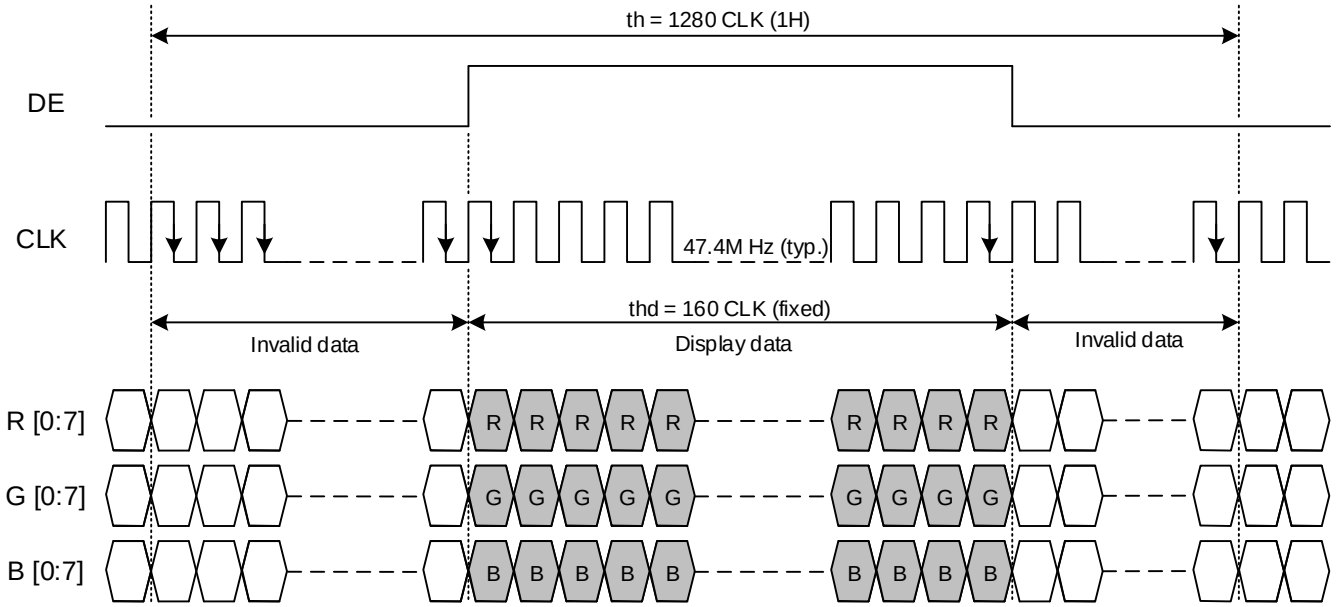


Fig. 8.1 Horizontal Timing

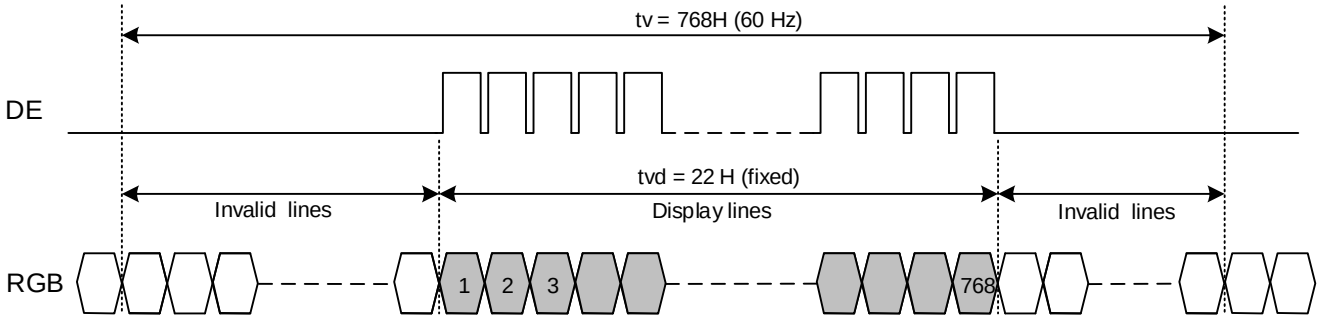


Fig. 8.2 Vertical Timing

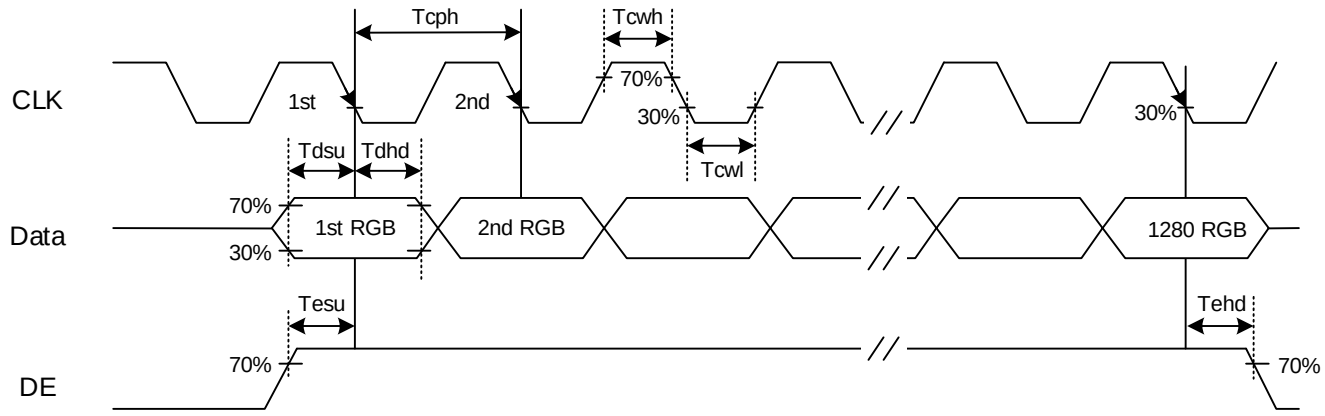


Fig. 8.3 Setup & Hold Time

8.5 TIME TABLE

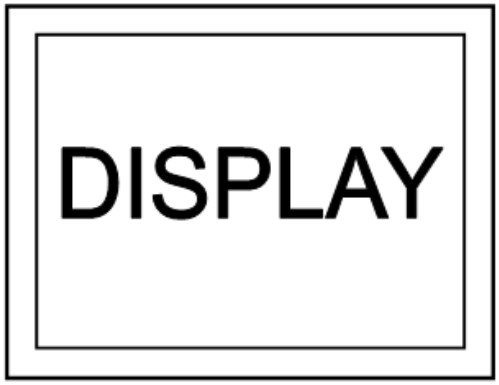
The column of timing sets including minimum, typical, and maximum as below are based on the best optical performance, frame frequency (Vsync) = 60 Hz to define. If 60 Hz is not the aim to set, less than 65 Hz for Vsync is recommended to apply for better performance by other parameter combination as the definitions in section 5.1.

A. Horizontal and Vertical Timing

Item		Symbol	Min.	Typ.	Max.	Unit
Horizontal	CLK Frequency	fclk	50	68.3	80	M Hz
	Display Data	thd		1280		CLK
	Cycle Time	th	1310	1440	-	
Vertical	Display Data	tvd		768		H
	Cycle Time	tv	771	790	-	

8.6 DISPLAY MODE CONTROL

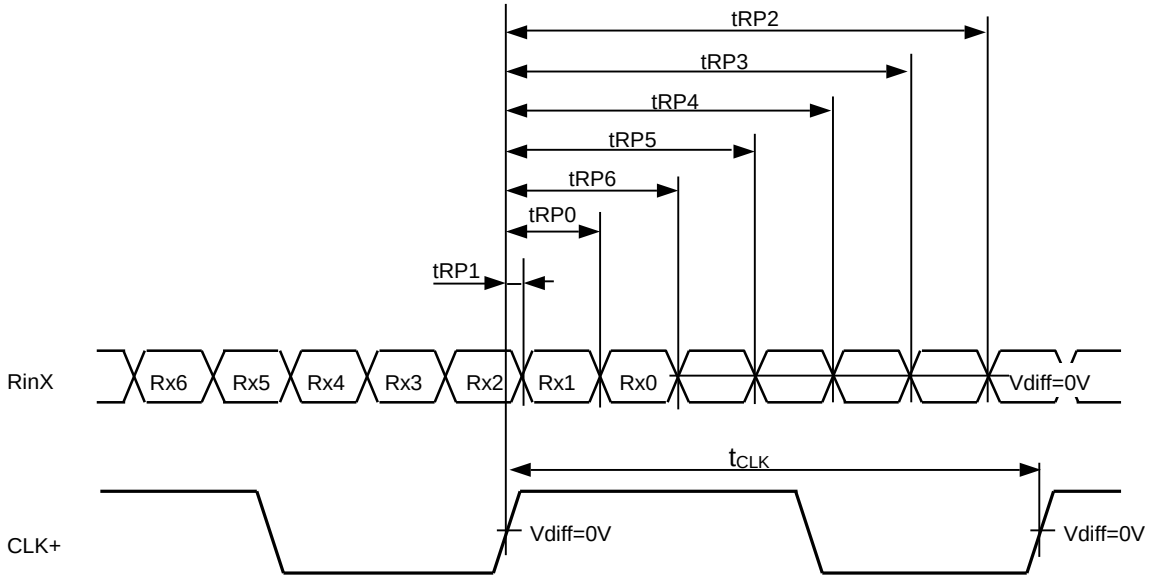
Scan direction is available to be switched as below by setting CN7's UD/ LR pin.



UD/LR : Low

UD/LR : High

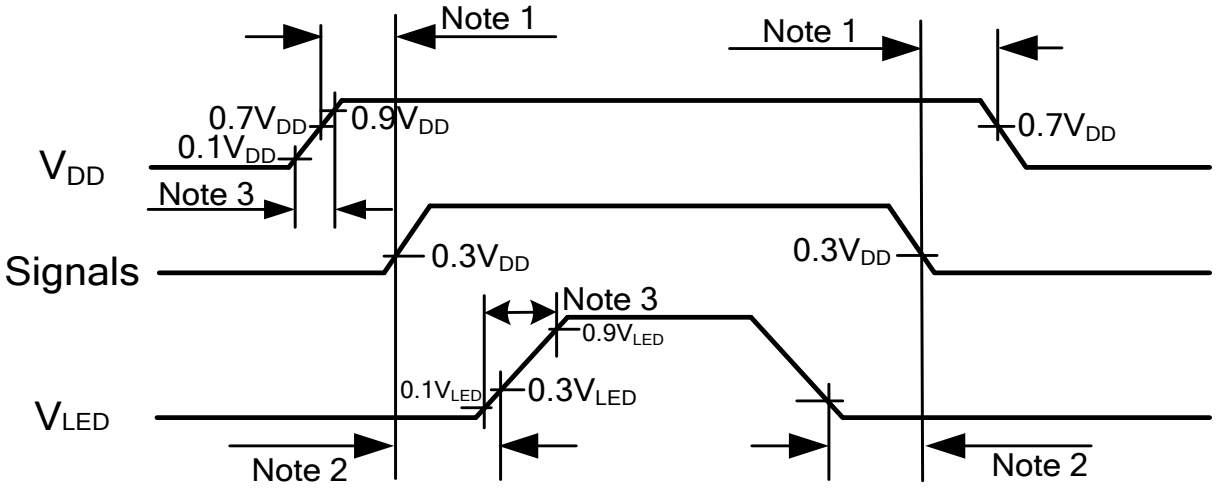
8.7 LVDS RECEIVER TIMING



RinX= (RinX+)-(RinX-) (X=0, 1, 2, 3)

Item		Symbol	Min.	Typ.	Max.	Unit
CLK	Cycle frequency	1/tcLK	50	68.3	(TBD)	MHz
RinX (X=0,1,2,3)	0 data position	tRP0	$1/7t_{CLK}$-0.65	$1/7*t_{CLK}$	$1/7t_{CLK}$+0.65	ns
	1st data position	tRP1	-0.65	0	-0.65	
	2nd data position	tRP2	$6/7t_{CLK}$-0.65	$6/7*t_{CLK}$	$6/7t_{CLK}$+0.65	
	3rd data position	tRP3	$5/7t_{CLK}$-0.65	$5/7*t_{CLK}$	$5/7t_{CLK}$+0.65	
	4th data position	tRP4	$4/7t_{CLK}$-0.65	$4/7*t_{CLK}$	$4/7t_{CLK}$+0.65	
	5th data position	tRP5	$3/7t_{CLK}$-0.65	$3/7*t_{CLK}$	$3/7t_{CLK}$+0.65	
	6th data position	tRP6	$2/7t_{CLK}$-0.65	$2/7*t_{CLK}$	$2/7t_{CLK}$+0.65	

8.8 POWER SEQUENCE



Note 1: In order to avoid any damages, V_{DD} has to be applied before all other signals. The opposite is true for power off where V_{DD} has to be remained on until all other signals have been switch off. The recommended time period is 1 second.

Note 2: In order to avoid showing uncompleted patterns in transient state. It is recommended that switching the backlight on is delayed for 1 second after the signals have been applied. The opposite is true for power off where the backlight has to be switched off 1 second before the signals are removed.

Note 3: In order to avoid high Inrush current, V_{DD} rising time need to set more than 0.5ms.

8.9 DATA INPUT for DISPLAY COLOR

8.9.1 ISP 6 bit compatibility mode

Input color		Red Data						Green Data						Blue Data					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
		MSB					LSB	MSB					LSB	MSB					LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note 1: Definition of gray scale : Color(n) Number in parenthesis indicates gray scale level. Larger number corresponds to brighter level.

Note 2: Data Signal : 1 : High, 0 : Low

8.9.2 ISP 8 bit compatibility mode

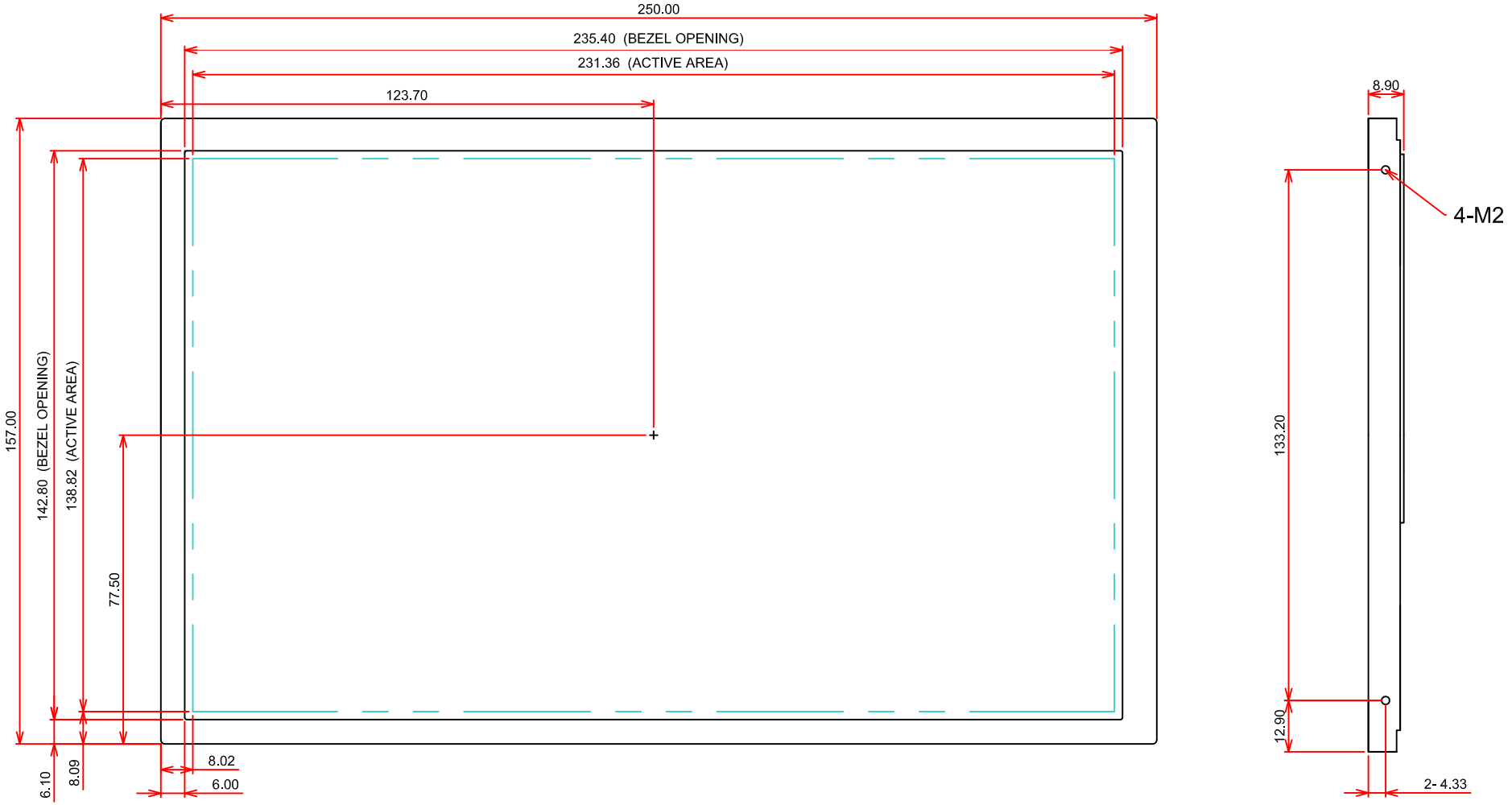
Input color		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
		MSB							LSB	MSB							LSB	MSB							LSB
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note 1: Definition of gray scale : Color(n) Number in parenthesis indicates gray scale level. Larger number corresponds to brighter level.

Note 2: Data Signal : 1 : High, 0 : Low

9. OUTLINE DIMENSIONS

9.1 FRONT VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

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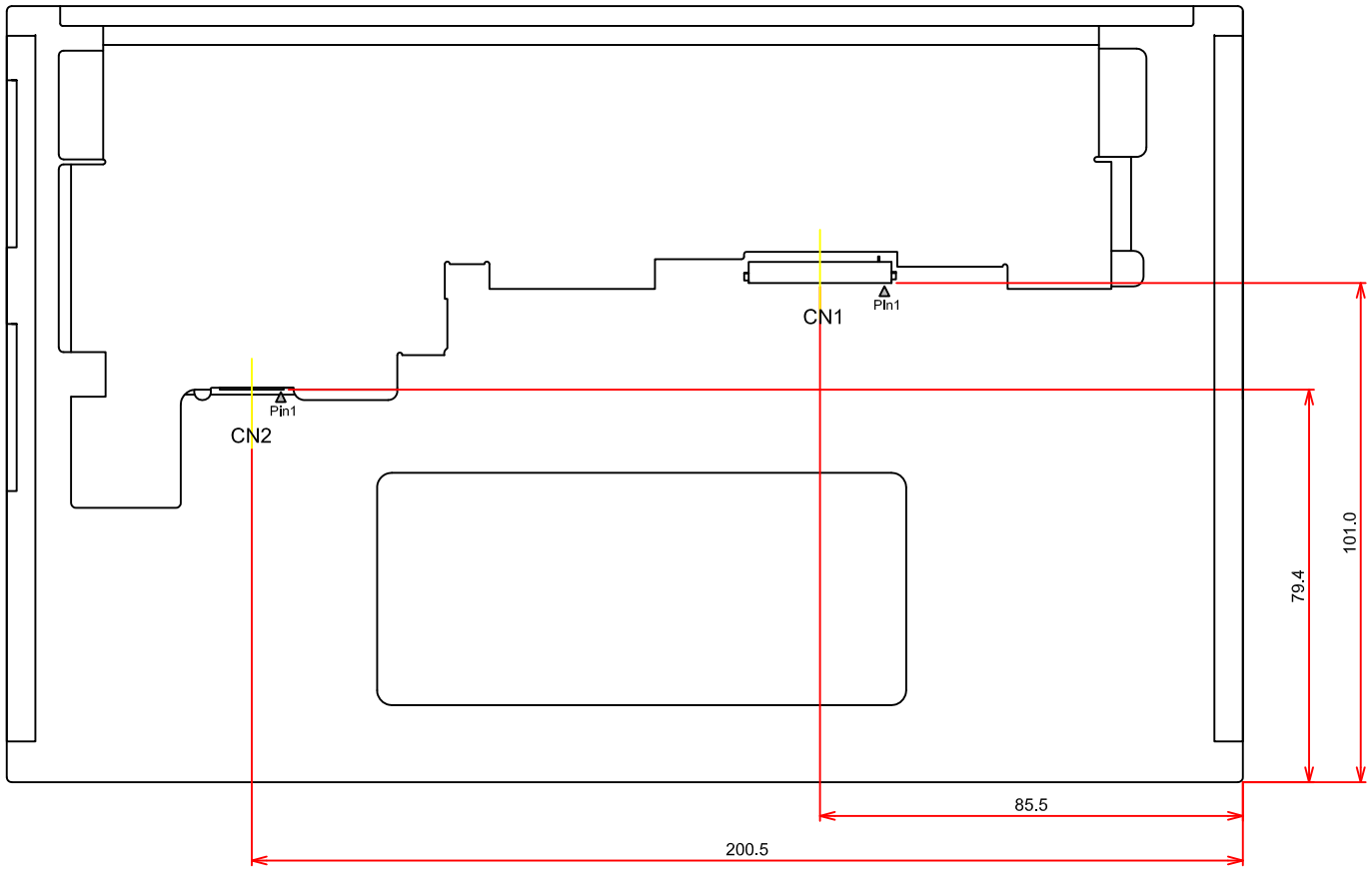
9.2 REAR VIEW



General Tolerance:±0.5mm
Scale : NTS
Unit : mm

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9. DESIGNATION of LOT MARK

1) The lot mark is showing in Fig.10.1. First 4 digits are used to represent production lot, T represented made in Taiwan, and the last 6 digits are the serial number.

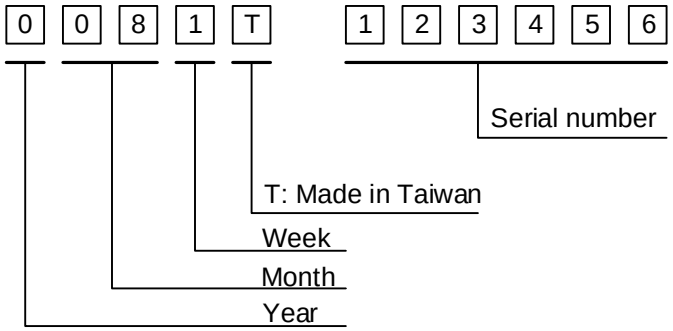

Fig. 10.1

2) The tables as below are showing what the first 4 digits of lot mark are shorted for.

Year	Lot Mark
2020	0
2021	1
2022	2
2023	3
2024	4

Month	Lot Mark	Month	Lot Mark
Jan.	01	Jul.	07
Feb.	02	Aug.	08
Mar.	03	Sep.	09
Apr.	04	Oct.	10
May	05	Nov.	11
Jun.	06	Dec.	12

Week	Lot Mark
1~7 days	1
8~14 days	2
15~21 days	3
22~28 days	4
29~31 days	5

3) The location of the lot mark is on the back of the display shown in Fig. 10.2

Label example :

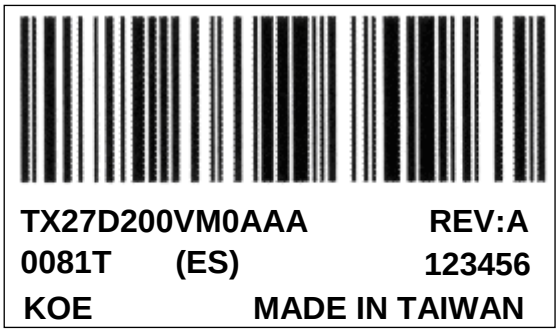

Fig. 10.2

Our company network supports you worldwide with offices in Germany, Austria, Switzerland, the UK and the USA. For more information please contact:

Headquarters

Germany

FORTEC Elektronik AG
Augsburger Str. 2b
82110 Germering

Phone: +49 89 894450-0
E-Mail: info@fortecag.de
Internet: www.fortecag.de

Fortec Group Members

Austria

Distec GmbH Office Vienna
Nuschinggasse 12
1230 Wien

Phone: +43 1 8673492-0
E-Mail: info@distec.de
Internet: www.distec.de

Germany

Distec GmbH
Augsburger Str. 2b
82110 Germering

Phone: +49 89 894363-0
E-Mail: info@distec.de
Internet: www.distec.de

Switzerland

ALTRAC AG
Bahnhofstraße 3
5436 Würenlos

Phone: +41 44 7446111
E-Mail: info@altrac.ch
Internet: www.altrac.ch

United Kingdom

Display Technology Ltd.
Osprey House, 1 Osprey Court
Hichingbrooke Business Park
Huntingdon, Cambridgeshire, PE29 6FN

Phone: +44 1480 411600
E-Mail: info@displaytechnology.co.uk
Internet: www. displaytechnology.co.uk

USA

Apollo Display Technologies, Corp.
87 Raynor Avenue,
Unit 1Ronkonkoma,
NY 11779

Phone: +1 631 5804360
E-Mail: info@apollodisplays.com
Internet: www.apollodisplays.com